

LLW-1/LGG-1 Schematics

Sandy Bridge

Cougar Point

2011-01-18

REV : -1

DY:None Installed

UMA:UMA platform installed only

PX:Discrete(both Robson and Whistler) SKU installed

RBS:Robson SKU installed only

WTL:Whistler SKU installed only

SAMSUNG:Use SAMSUNG VRAM

Hynix:Use Hynix VRAM

VRAM_1G:Use 1G VRAM

VRAM_2G:Use 2G VRAM

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

LLW-1 / LGG-1

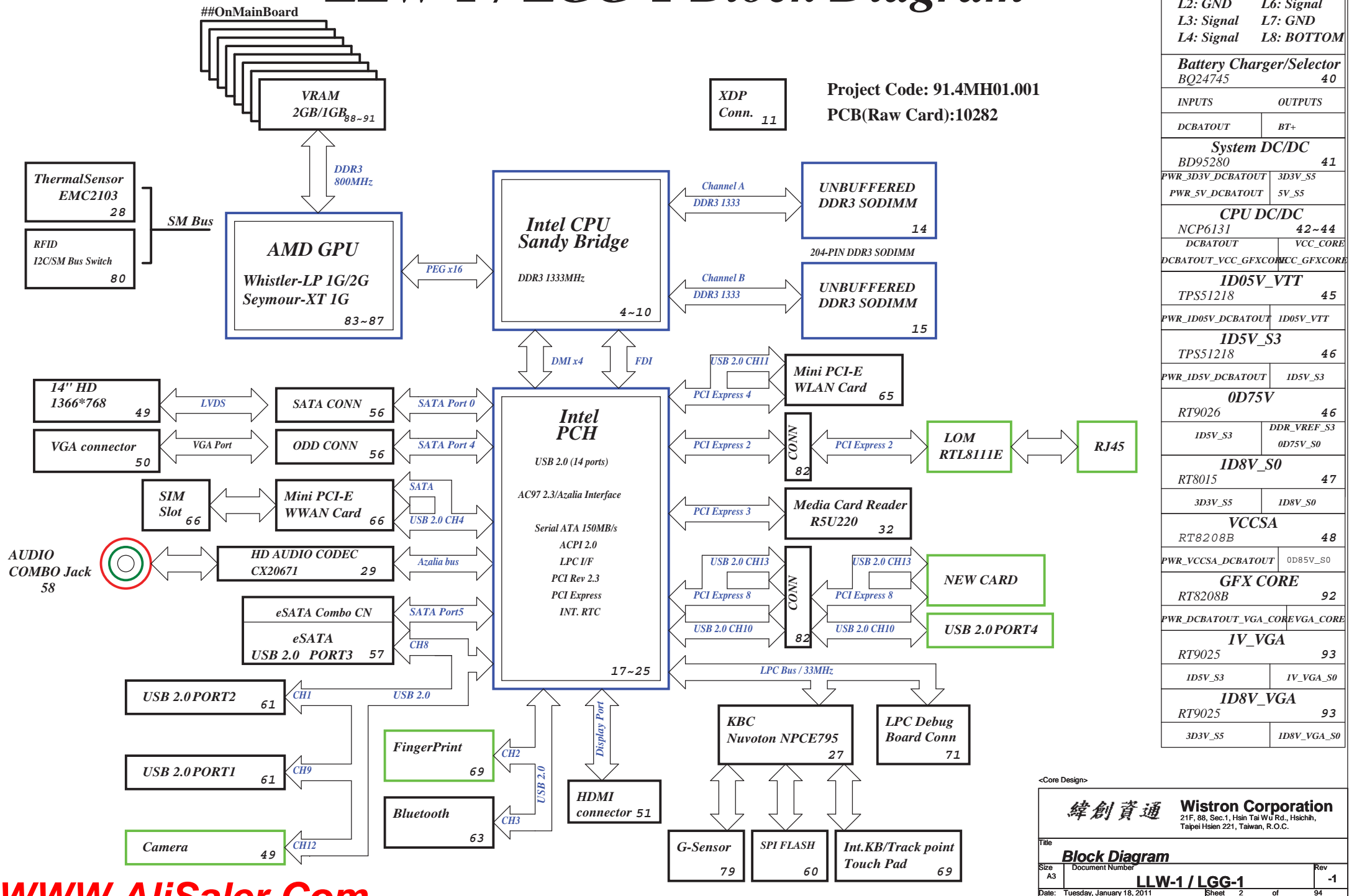
Rev

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Date: Tuesday, January 18, 2011

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LLW-1 / LGG-1 Block Diagram



Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

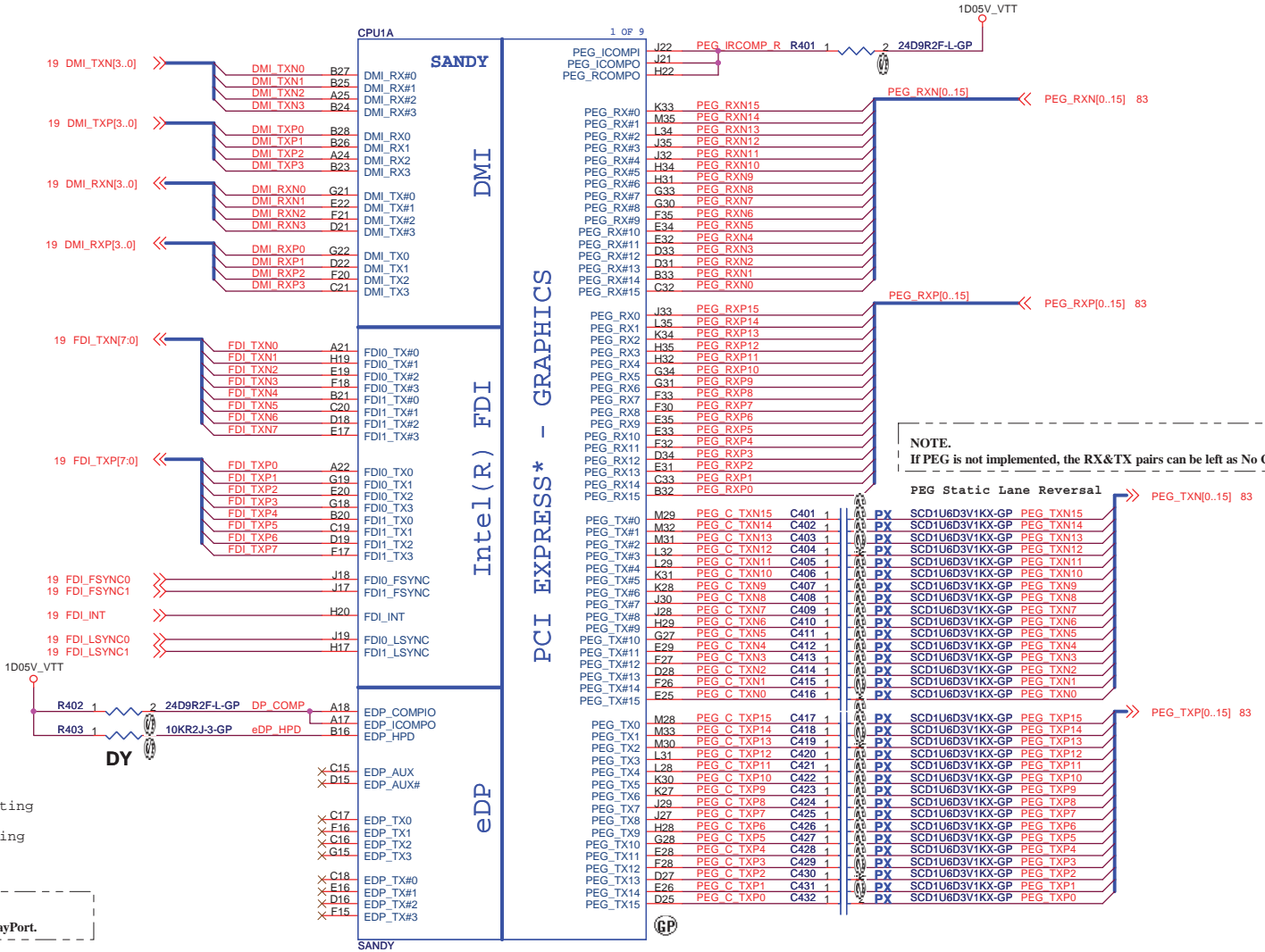


Table 4.1- Central Processing Unit slot multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
FOXCONN	PZ98827-364B-41F	N/A	62.10055.421
TYCO	2-2013620-3	N/A	62.10040.771

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Title

CPU (PCIE/DMI/FDI)

Size

A3

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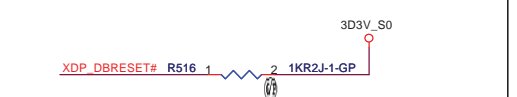
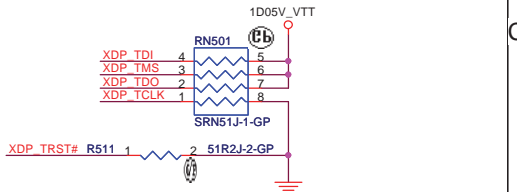
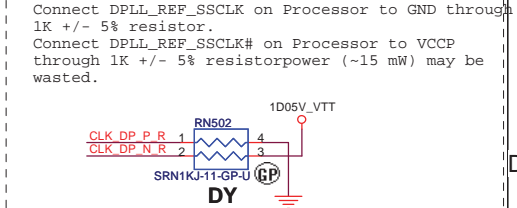


Table 5.1- N-Channel MOSFET multi-source

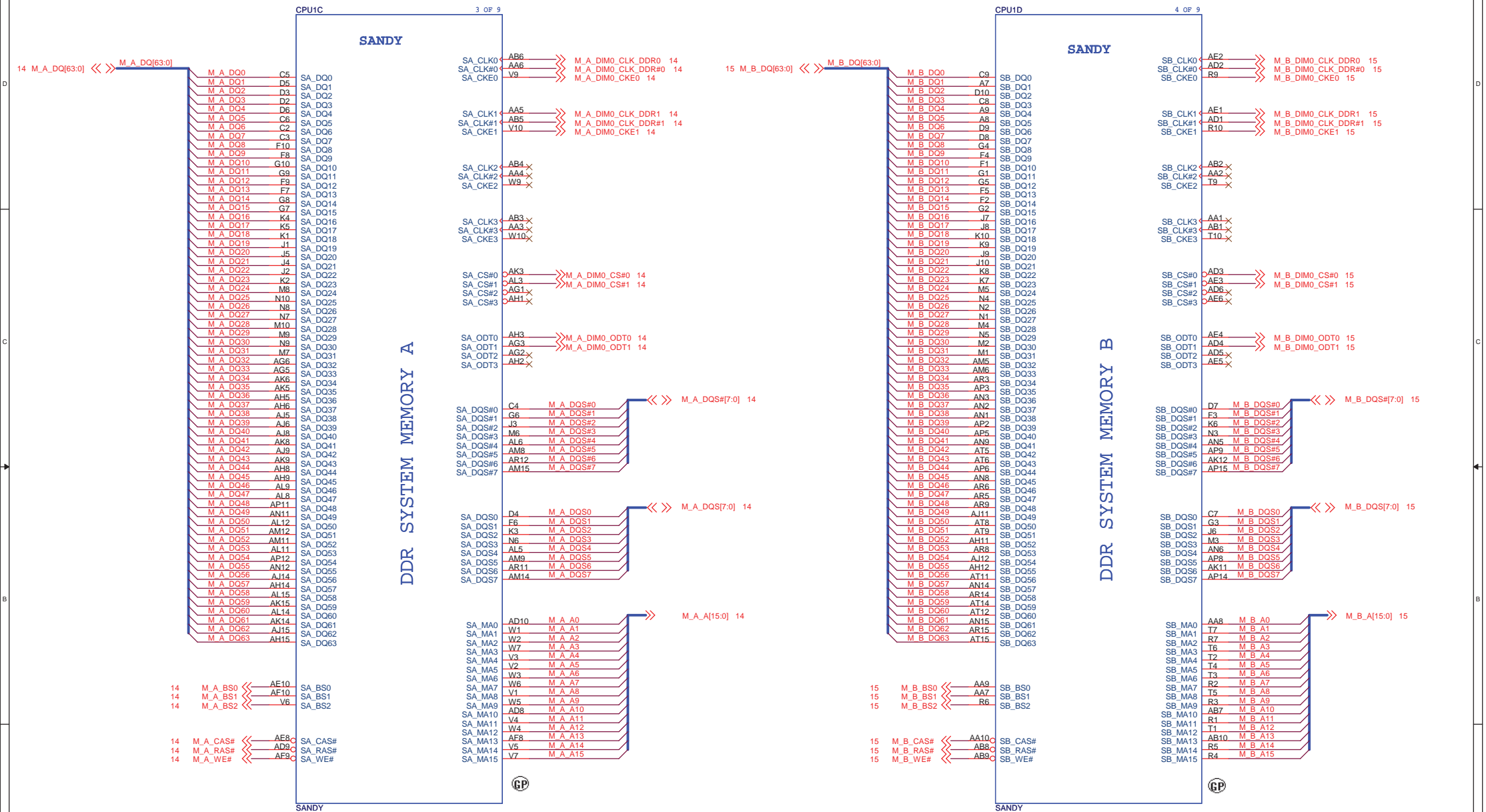
Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002K	N/A	84.2N702.J31
DIODES	2N7002K	N/A	84.2N702.031
NXP	2N7002BK	N/A	84.07002.I31

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Title			
CPU (Thermal/CLK/PM)			
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SSID = CPU

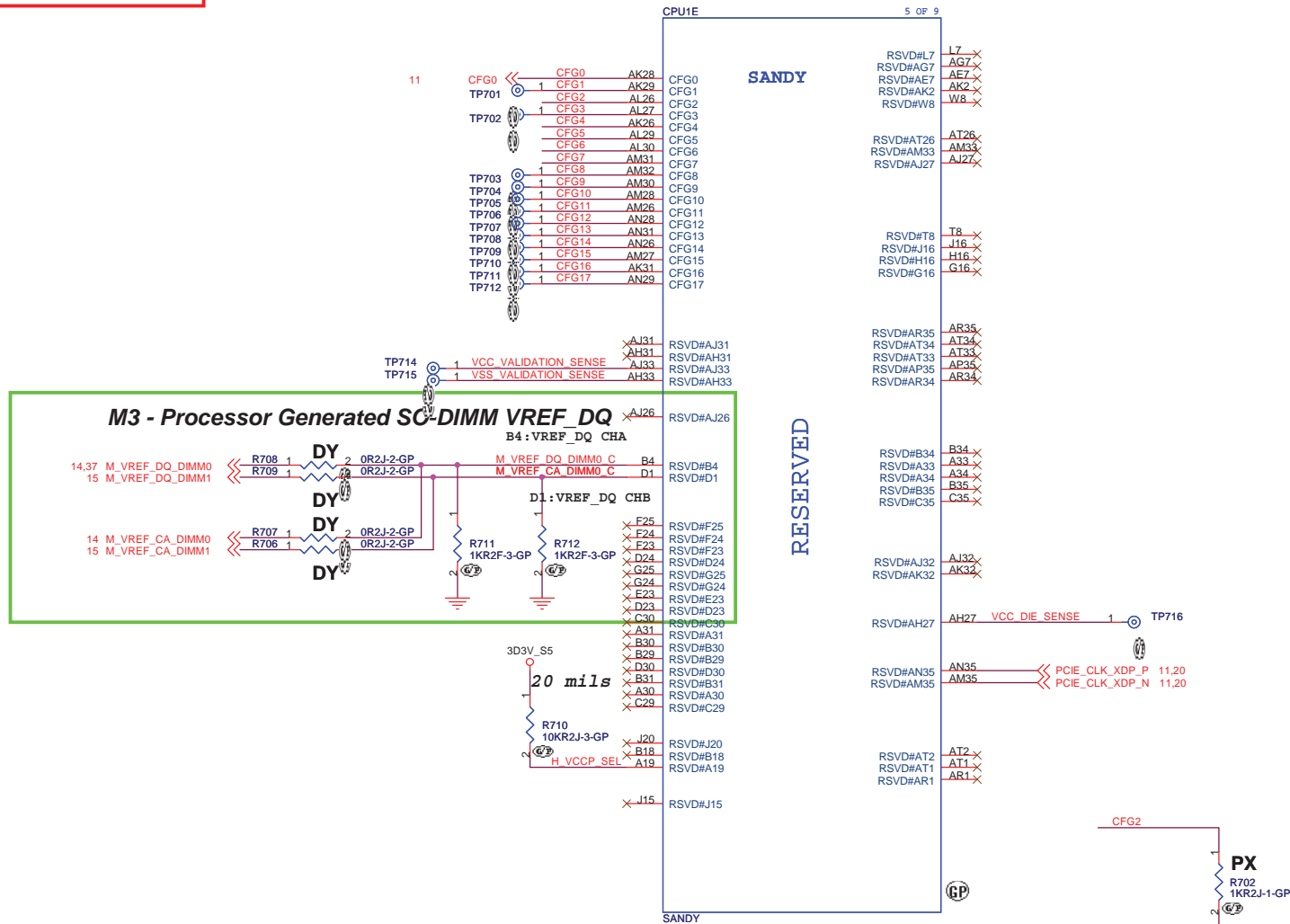


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Title		CPU (DDR)	
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SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

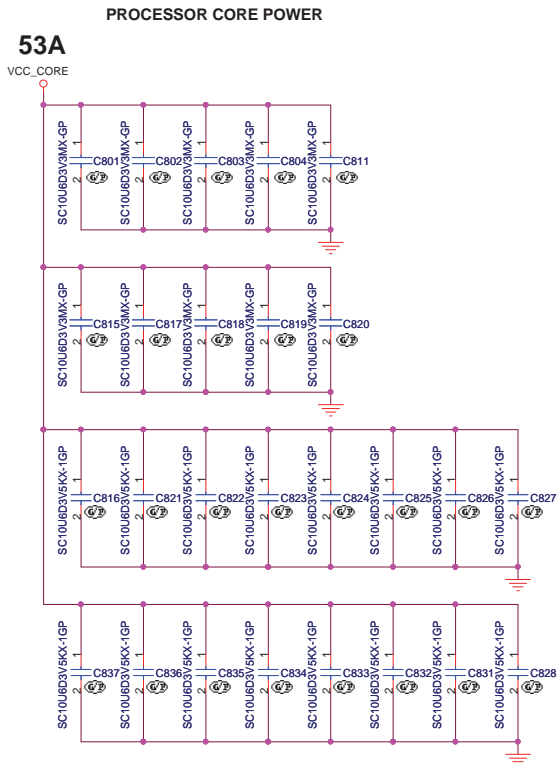
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

<Core Design>	
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Title	CPU (RESERVED)
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SSID = CPU



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AC35 VCC
AC34 VCC
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AC32 VCC
AC31 VCC
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AC29 VCC
AC28 VCC
AC27 VCC
AC26 VCC
AA35 VCC
AA34 VCC
AA33 VCC
AA32 VCC
AA31 VCC
AA30 VCC
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U35 VCC
U34 VCC
U33 VCC
U32 VCC
U31 VCC
U30 VCC
U29 VCC
U28 VCC
U27 VCC
U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

SANDY

POWER

SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

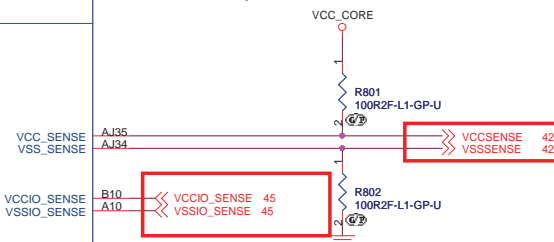
VCCIO_AH13 VCC
VCCIO_AH10 VCC
VCCIO_AG10 VCC
VCCIO_AG10 VCC
VCCIO_Y10 VCC
VCCIO_U10 VCC
VCCIO_P10 VCC
VCCIO_L14 VCC
VCCIO_J14 VCC
VCCIO_J13 VCC
VCCIO_J12 VCC
VCCIO_J11 VCC
VCCIO_H14 VCC
VCCIO_H12 VCC
VCCIO_H11 VCC
VCCIO_G14 VCC
VCCIO_G13 VCC
VCCIO_G12 VCC
VCCIO_F14 VCC
VCCIO_F13 VCC
VCCIO_F12 VCC
VCCIO_F11 VCC
VCCIO_E14 VCC
VCCIO_E12 VCC

VCCIO_E11 VCC
VCCIO_D14 VCC
VCCIO_D13 VCC
VCCIO_D12 VCC
VCCIO_D11 VCC
VCCIO_C14 VCC
VCCIO_C13 VCC
VCCIO_C12 VCC
VCCIO_C11 VCC
VCCIO_B14 VCC
VCCIO_B12 VCC
VCCIO_A14 VCC
VCCIO_A13 VCC
VCCIO_A12 VCC
VCCIO_A11 VCC
VCCIO_J23 VCC

VIDALERT#
VIDCLK#
VIDSOUT

AJ29 H_CPU_SVIDALRT# R803 1 2 43R2J-GP VR_SVID_ALERT# 42
AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 42
AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 42

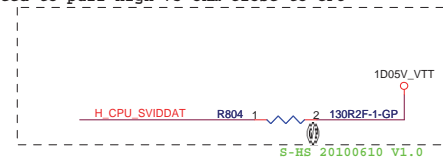
R801, R802 need to close to CPU



VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMPV7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



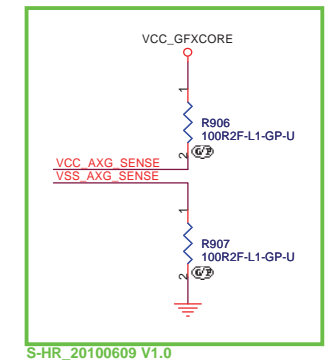
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Title
Size Custom
Date: Tuesday, January 18, 2011
CPU (VCC CORE)
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VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge
```

R906,R907 close to CPU



SENSE
LINES

VRFF

GRAPHICS

DDR3 -1.5V RAILS

SA RAIL

MISC

1.8V RAIL

SANDY

VCC_GFXCORE

PROCESSOR VAXG: 24A

VAXG_SENSE
VSSAXG_SENSE

AK35	VCC_AXG_SENSE	42
AK34	VSS_AXG_SENSE	42

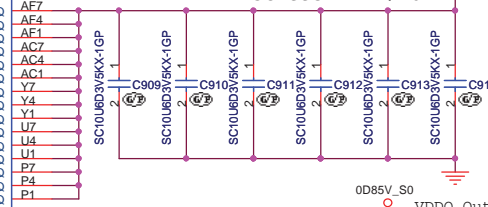
+V_SM_VREF_CNT should have 10 mil trace width

AL1 +V_SM_VREF_CNT << +V_SM_VREF_CNT 37

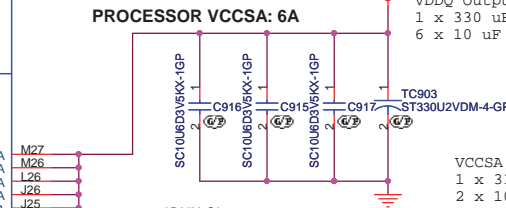
Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width. 18

[illegible]

PROCESSOR VDDQ: 10A



PROCESSOR VCCSA: 6A



VCCSA Output Decoupling Recommendation:
 1 x 330 uF
 2 x 10 uF at Bottom Socket Cavity
 1 x 10 uF at Bottom Socket Edge

R902 need be close to pin H23.

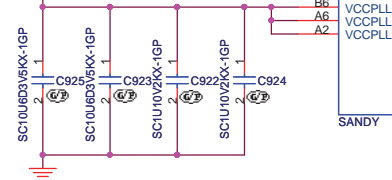
VCCSA_SENSE

FC_C22
VCCSA_VID1

RN901
SRN1KJ-7-GP

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

PROCESSOR VCCPLL: 1.2A

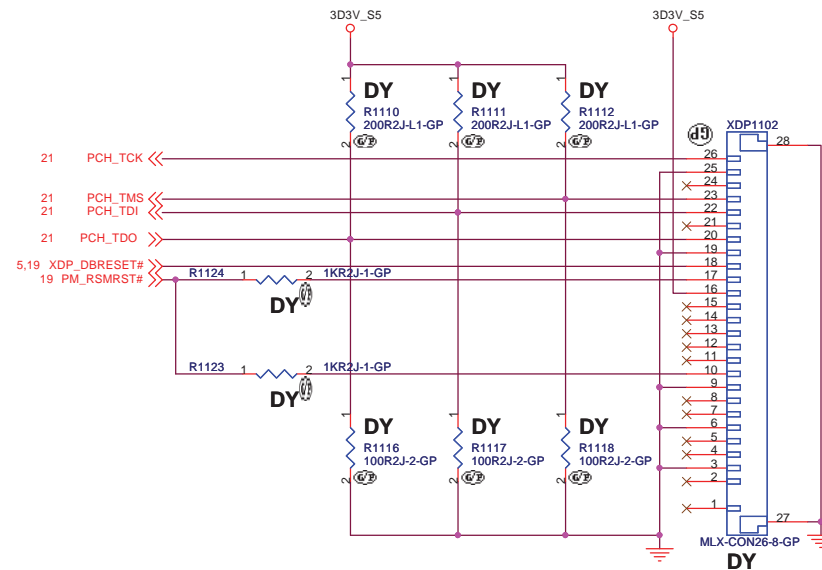
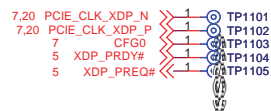


VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

<Core Design>

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Title			
CPU (VCC GFXCORE)			
Size A3	Document Number		Rev
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DEBUG Interface for Processor.

CPU XDP SFF 26pin IF
 Pin 1 OBSFN_A0 (PREQ#, I/O)
 Pin 2 OBSFN_A1 (PRDY#, I/O)
 Pin 3 GND
 Pin 4 OBSDATA_A0 (Open, I/O)
 Pin 5 OBSDATA_A1 (Open, I/O)
 Pin 6 GND
 Pin 7 OBSDATA_A2 (Open, I/O)
 Pin 8 OBSDATA_A3 (Open, I/O)
 Pin 9 GND
 Pin 10 HOOK0 (PWRGD, In)
 Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
 Pin 12 HOOK2 (CFG0, Out)
 Pin 13 HOOK3 (vr_READYSYS_PWROK, Out)
 Pin 14 HOOK4 (BCLK, In)
 Pin 15 HOOK5 (BCLK#, In)
 Pin 16 VCCOBS_AB (VCCP Voltage of CPU, In)
 Pin 17 HOOK6 (RESET#, Out)
 Pin 18 HOOK7 (DBR#, Out)
 Pin 19 GND
 Pin 20 TDO, In
 Pin 21 TRST#, Out
 Pin 22 TDI, Out
 Pin 23 TMS, Out
 Pin 24 TCK1 (Open)
 Pin 25 GND
 Pin 26 TCK0 ,Out

TABLE

PCH PIN	REF DES	PCH ES1 JTAG		PCH ES2 JTAG		PRODUCTION	
		Enable	Disable	Enable	Disable	Enable	Disable
TDO	R1110	DY	DY	200 Ohms	DY	DY	DY
	R1116	DY	DY	100 Ohms	DY	DY	DY
	R2	DY	DY	DY	DY	51 Ohms	DY
TMS	R1112	200 Ohms	DY	200 Ohms	DY	DY	DY
	R1118	100 Ohms	DY	100 Ohms	DY	DY	DY
	R91	DY	DY	DY	DY	51 Ohms	DY
TDI	R1111	200 Ohms	20K Ohms	200 Ohms	DY	DY	DY
	R1117	100 Ohms	10K Ohms	100 Ohms	DY	DY	DY
	R90	DY	DY	DY	DY	51 Ohms	DY
TCK	R541	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms
TRST#	R953	20K Ohms	DY	DY	DY	DY	DY
	R535	10K Ohms	DY	DY	DY	DY	DY
	R103	DY	DY	DY	DY	DY	DY

↑
LOGIC

DEBUG Interface for PCH.

PCH XDP SFF 26pin IF
 Pin 1 OBSFN_A0 (Open, I/O)
 Pin 2 OBSFN_A1 (Open, I/O)
 Pin 3 GND
 Pin 4 OBSDATA_A0 (Open, I/O)
 Pin 5 OBSDATA_A1 (Open, I/O)
 Pin 6 GND
 Pin 7 OBSDATA_A2 (Open, I/O)
 Pin 8 OBSDATA_A3 (Open, I/O)
 Pin 9 GND
 Pin 10 HOOK0 (RSMRST#, In)
 Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
 Pin 12 HOOK2 (Open)
 Pin 13 HOOK3 (Open)
 Pin 14 HOOK4 (Open)
 Pin 15 HOOK5 (Open)
 Pin 16 VCCOBS_AB (3.3VSUS, In)
 Pin 17 HOOK6 (RSMRST#, Out)
 Pin 18 HOOK7 (DBR#, Out)
 Pin 19 GND
 Pin 20 TDO (JTAG, In)
 Pin 21 TRST# (Open)
 Pin 22 TDI (JTAG, Out)
 Pin 23 TMS (JTAG, Out)
 Pin 24 TCK1 (Open)
 Pin 25 GND
 Pin 26 TCK0 (JTAG, Out)

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Title XDP CONN	
Size A3	Document Number LLW-1 / LGG-1
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
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Title

CLOCK GEN

Size
A4

Document Number

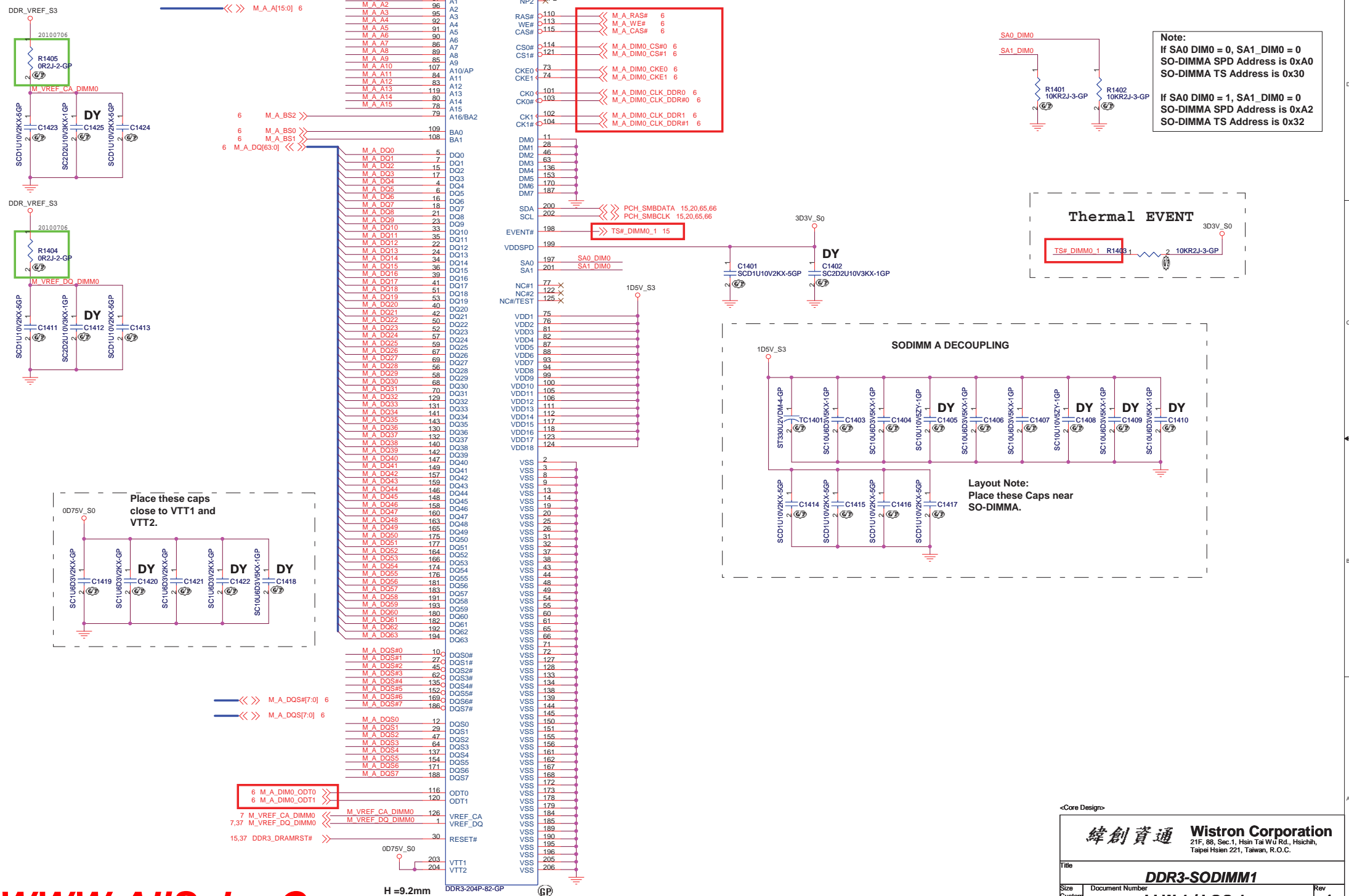
LLW-1 / LGG-1

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SSID = MEMORY



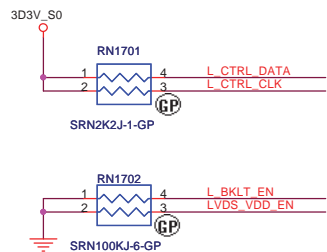
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Title <div>DDR3-SODIMM2</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
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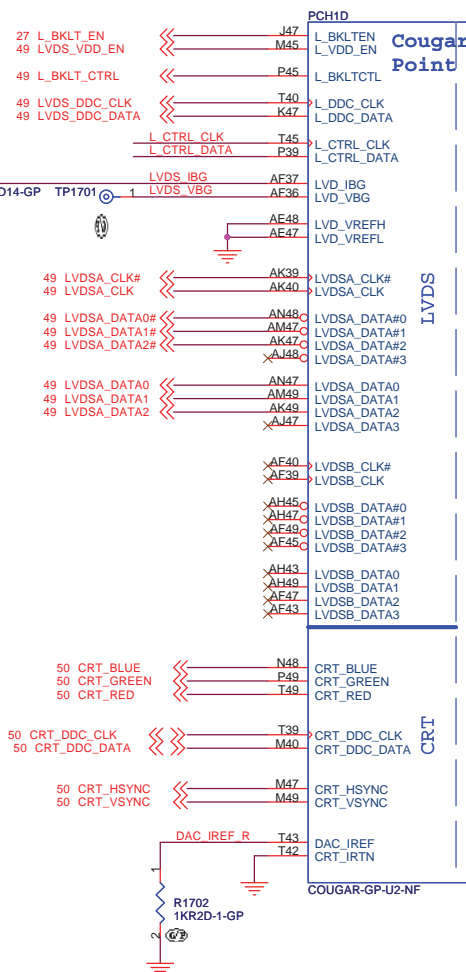
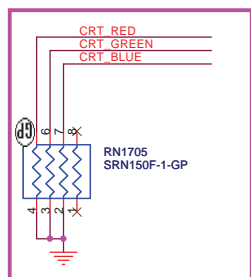


L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display

Place near PCH

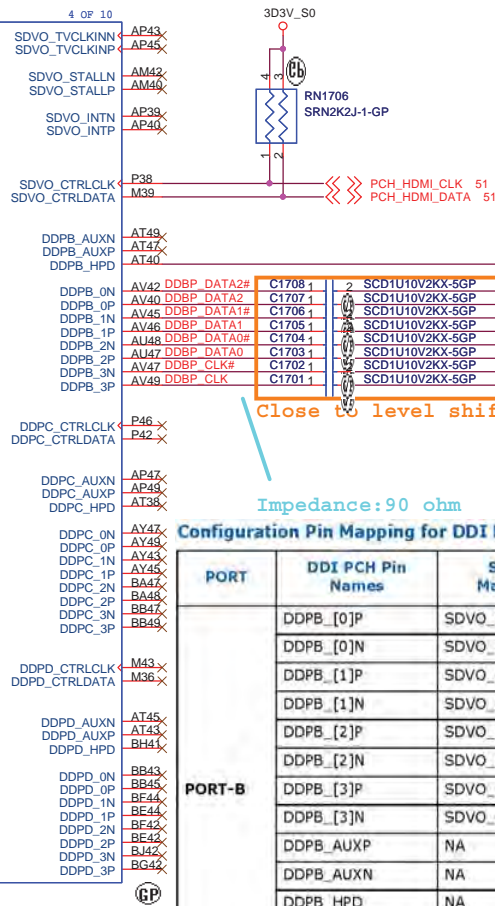
Impedance:90 ohm

Close to PCH side



Digital Display Interface

Cougar Point



DDI Port B Detect:(SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected

Close to level shifter side

Impedance:90 ohm

Impedance:100 ohm

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

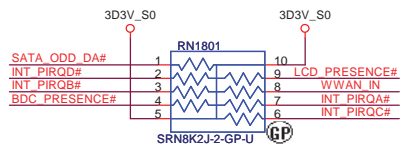
PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPDP	NA	DDPB_HPDP	HDMI_B_HPDP
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI_B_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI_B_CTRLDATA

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Title	PCH (LVDS/CRT/DDI)		
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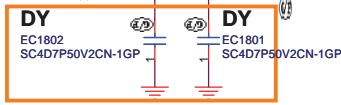
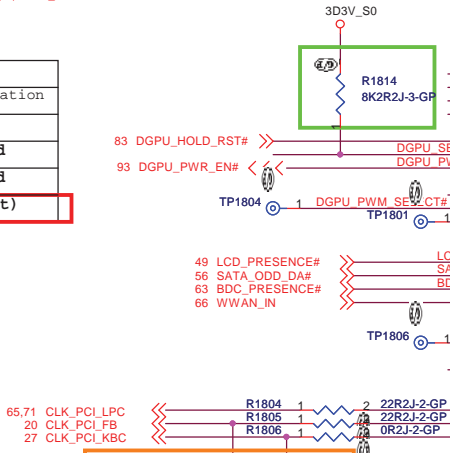
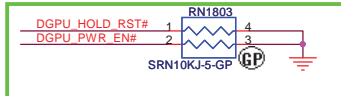
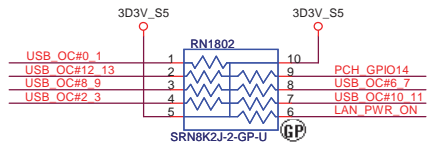
SSID = PCH



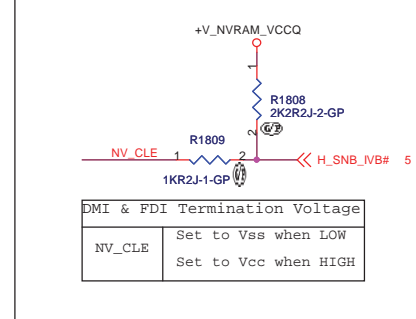
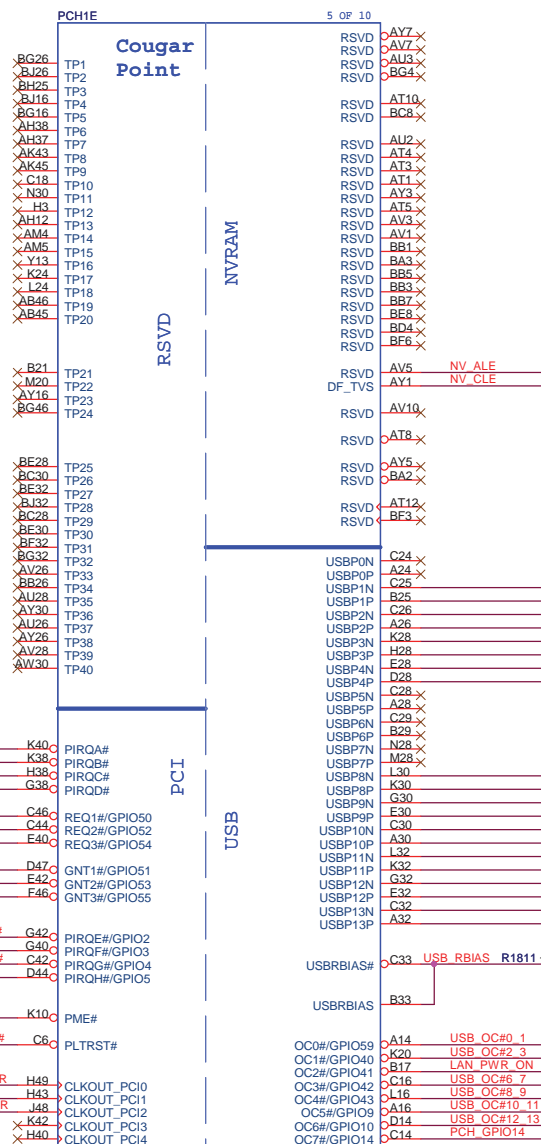
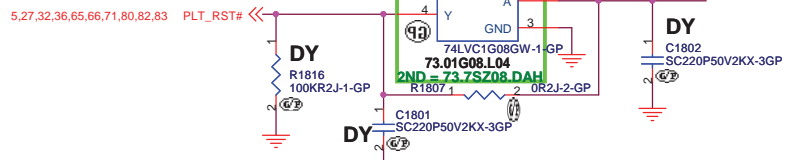
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

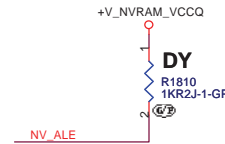


KBC CLK EMI

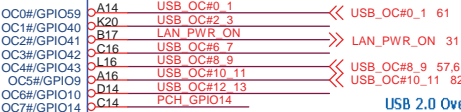


DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Danbury Technology:
Disabled when Low.
Enable when High.



USB	
Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card



USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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Taipei Hsien 221, Taiwan, R.O.C.

PCH (PCI/USB/NVRAM)			
Size A3	Document Number	Rev	-1
Date: Tuesday, January 18, 2011	Sheet 18 of 94		

SSID = PCH

4 DMI_RXN[3..0] <<>=
4 DMI_RXP[3..0] <<>=
4 DMI_TXN[3..0] <<>=
4 DMI_TXP[3..0] <<>=

FDI_TXN[7..0] 4
FDI_TXP[7..0] 4

Deep S4/S5 Supported

Deep S4/S5 Not Supported

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.

4 DMI_RXN3 >>> BC24
4 DMI_RXN2 >>> BE20
4 DMI_RXN1 >>> BG18
4 DMI_RXN0 >>> BG20
4 DMI_RXP3 >>> BE24
4 DMI_RXP2 >>> BC20
4 DMI_RXP1 >>> BJ18
4 DMI_RXP0 >>> BJ20
4 DMI_TXN3 >>> AW24
4 DMI_TXN2 >>> AW20
4 DMI_TXN1 >>> BB18
4 DMI_TXN0 >>> AV18
4 DMI_TXP3 >>> AY24
4 DMI_TXP2 >>> AY20
4 DMI_TXP1 >>> AY18
4 DMI_TXP0 >>> AU18

PCH1C

3 OF 10

Cougar
Point

DMI

FDI

FDI_RXN0 >>> BJ14
FDI_RXN1 >>> AY14
FDI_RXN2 >>> BE14
FDI_RXN3 >>> BH13
FDI_RXN4 >>> BJ12
FDI_RXN5 >>> BG10
FDI_RXN6 >>> BG9
FDI_RXN7 >>> BH9
FDI_RXP0 >>> BG14
FDI_RXP1 >>> BB14
FDI_RXP2 >>> BG13
FDI_RXP3 >>> BE12
FDI_RXP4 >>> BG12
FDI_RXP5 >>> BJ10
FDI_RXP6 >>> BJ10
FDI_RXP7 >>> BH9
FDI_TXN7 >>> FDI_TXN7 4
FDI_TXN6 >>> FDI_TXN6 4
FDI_TXN5 >>> FDI_TXN5 4
FDI_TXN4 >>> FDI_TXN4 4
FDI_TXN3 >>> FDI_TXN3 4
FDI_TXN2 >>> FDI_TXN2 4
FDI_TXN1 >>> FDI_TXN1 4
FDI_TXN0 >>> FDI_TXN0 4
FDI_TXP7 >>> FDI_TXP7 4
FDI_TXP6 >>> FDI_TXP6 4
FDI_TXP5 >>> FDI_TXP5 4
FDI_TXP4 >>> FDI_TXP4 4
FDI_TXP3 >>> FDI_TXP3 4
FDI_TXP2 >>> FDI_TXP2 4
FDI_TXP1 >>> FDI_TXP1 4
FDI_TXP0 >>> FDI_TXP0 4

FDI_INT >>> AW16
FDI_FSYNCO >>> AV12
FDI_FSYNC1 >>> BC10
FDI_LSYNCO >>> AV14
FDI_LSYNC1 >>> BB10
FDI_INT 4
FDI_FSYNCO 4
FDI_FSYNC1 4
FDI_LSYNCO 4
FDI_LSYNC1 4

DSWVRMEN

DPWROK

WAKE#

CLKRUN#/GPIO32

SUS_STAT#/GPIO61

SUSCLK#/GPIO62

SLP_S5#/GPIO63

SLP_S4#

SLP_S3#

SLP_A#

SLP_SUS#

PMSYNCH

SLP_LAN#/GPIO29

A18 DSWODVREN

E22 PCH DPWROK

B9 PCIE WAKE#

N3 PM_CLKRUN#

G8 PM_SUS_STAT#

N14 SUS_CLK

D10 PM_SLP_S5#

H4 SLP_S4# R

E4 SLP_S3# R

G10 PM_SLP_A#

G16 PM_SLP_SUS#

AP14 H_PM_SYNC

K14 PM_SLP_LAN#

TP1901 TPAD14-GP

TP1902 TPAD14-GP

TP1903 TPAD14-GP

TP1904 TPAD14-GP

TP1905 TPAD14-GP

TP1906 TPAD14-GP

TP1907 TPAD14-GP

TP1908 TPAD14-GP

TP1909 TPAD14-GP

TP1910 TPAD14-GP

TP1911 TPAD14-GP

TP1912 TPAD14-GP

TP1913 TPAD14-GP

TP1914 TPAD14-GP

TP1915 TPAD14-GP

TP1916 TPAD14-GP

TP1917 TPAD14-GP

TP1918 TPAD14-GP

TP1919 TPAD14-GP

TP1920 TPAD14-GP

TP1921 TPAD14-GP

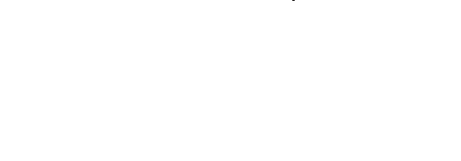
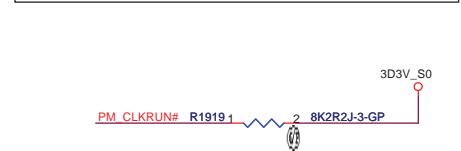
TP1922 TPAD14-GP

VccDSW3_3
DPWROK
VccSUS3_3
RSMRST#

For platforms not supporting Deep S4/S5

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	PCH (DMI/FDI/PM)	
Size A3	Document Number	Rev
	LLW-1 / LGG-1	-1
Date: Tuesday, January 18, 2011	Sheet 19	of 94

WWW.AliSaler.Com

SSID = PCH

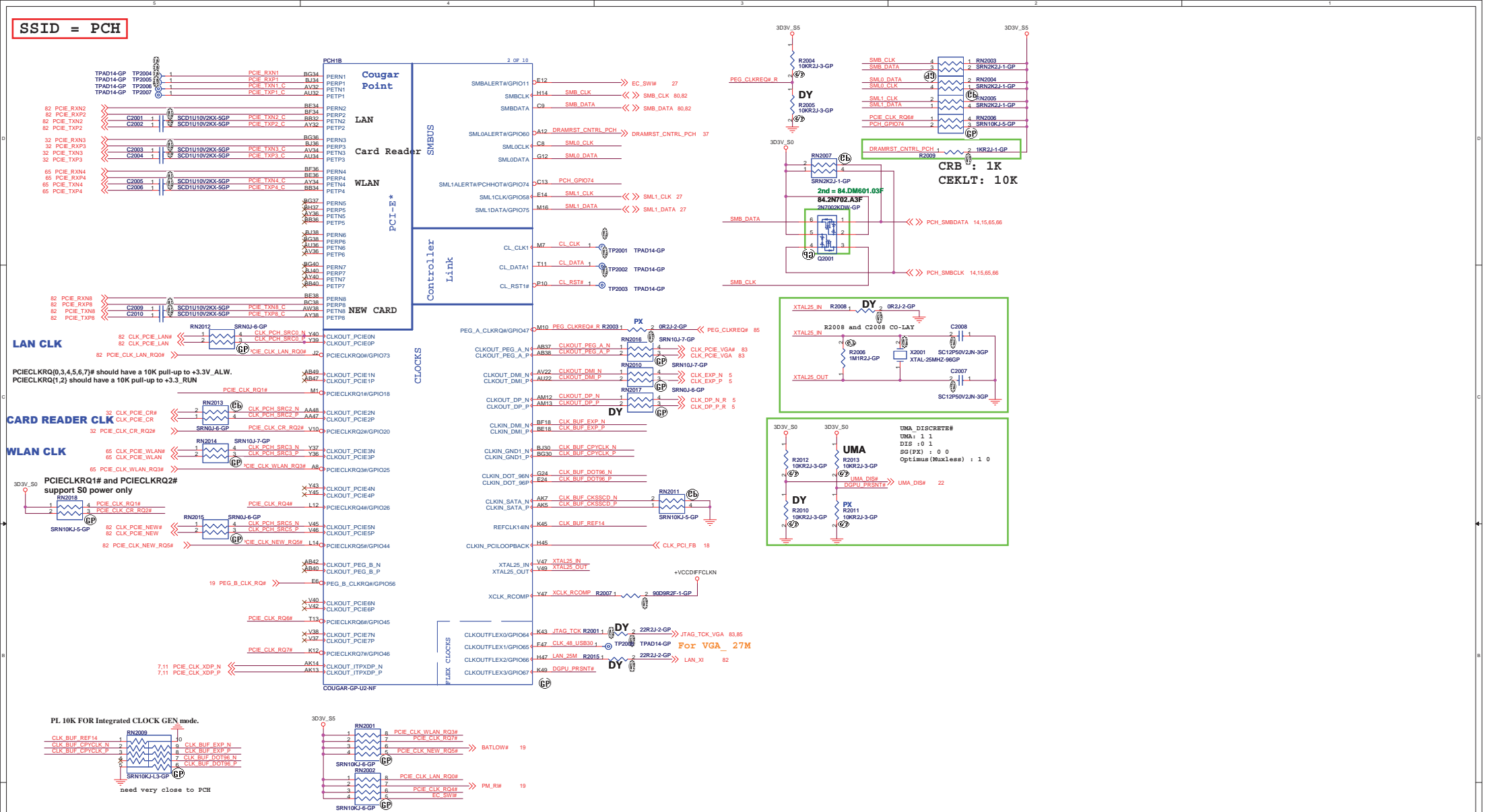


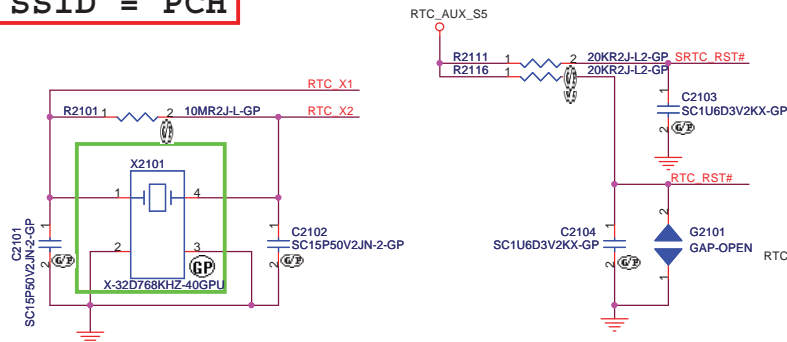
Table 20.1- Dual N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002KDW	N/A	84.2N702.A3F
DIODES	DMN601DWK-7	N/A	84.DM601.03F
NXP	2N7002BKS	N/A	84.2N702.E3F

«Core Design»

Wistron Corporation			
21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.			
PCH (PCI-E/SMBUS/CLOCK/CL)			
File	Document Number	Rev	
Size	LLW-1 / LGG-1	-1	
Date	Tuesday, January 18, 2011	Sheet	20 of 94

SSID = PCH



29 HDA_CODEC_SYNC <<< 0R2J-2-GP 2 1R2122 HDA_SYNC
29 HDA_CODEC_SDOOUT <<< 0R2J-2-GP 2 1R2123 HDA_SDOOUT

29 HDA_CODEC_RST# <<< 2 1R2102 HDA_RST#
29 HDA_CODEC_BITCLK <<< 1 1R2102 HDA_BITCLK

Flash Descriptor Security Override	
HDA_SDOOUT	Low = Default High = Enable

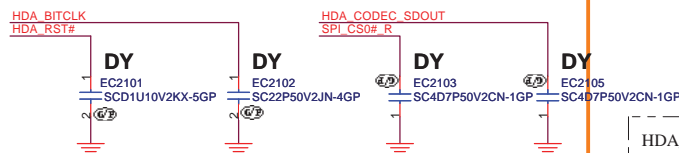
NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

+3VS_+1.5VS_HDA_IO
R2103 1 2 1KR2J-1-GP HDA_SYNC
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

For EMI



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

27 ME_UNLOCK <<< R2107 1 2 1KR2J-1-GP HDA_SDOOUT A36
TPAD14-GP TP2105 1 PCH_GPIO33 C36
X N32C

11 PCH_TCK >>> PCH_TCK J3
11 PCH_TMS >>> J7
11 PCH_TDI >>> K5
11 PCH_TDO <<< H1

27,60 SPL_CLK_R <<< T3
27,60 SPL_CS0#_R <<< SPI_CS0#_R Y14
X T1C

27,60 SPI_SL_R <<< V4
27,60 SPI_SO_R >>> U3

22 PSW_CLR#
22 MFG1_MODE
22 S_GPIO

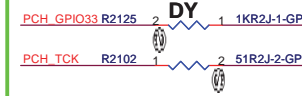
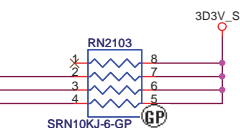
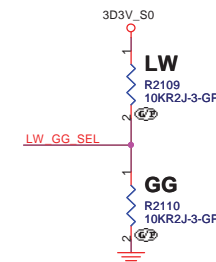


Table 21.1 Project_ID

	LW_GG_SEL
LW	High
GG	LOW



1 OF 10
PCH1A
RTCX1 A20
RTCX2 C20
RTC_RST# D20
SRTC_RST# G22
SM_INTRUDER# K22
PCH_INTRVREM# C17
INTVRMEN

LPC
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#GPIO23
SERIRQ

LPC_AD[0..3] <<< LPC_AD[0..3] 27,65,71
LPC_FRAME# 27,65,71
LW_GG_SEL
INT_SERIRQ 22,27

SATA 6G
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP

AM3 >>> SATA_RXN0 56
AM1 >>> SATA_RXP0 56
AP7 >>> SATA_TXN0 56
AP5 >>> SATA_TXP0 56
AM10 >>> SATA_RXN1 66
AM8 >>> SATA_RXP1 66
AP11 >>> SATA_TXN1 66
AP10 >>> SATA_TXP1 66
AD7 >>> SATA_RXN4 56
AD5 >>> SATA_RXP4 56
AH5 >>> SATA_TXN4 56
AH4 >>> SATA_TXP4 56
Y7 >>> SATA_RXN5 57
Y5 >>> SATA_RXP5 57
AD3 >>> SATA_TXN5 57
AD1 >>> SATA_TXP5 57
Y3 >>> SATA_RXN6 57
Y1 >>> SATA_RXP6 57
AB3 >>> SATA_TXN6 57
AB1 >>> SATA_TXP6 57

SATA 6G
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

SATA 6G
SATA6RXN
SATA6RXP
SATA6TXN
SATA6TXP
SATA7RXN
SATA7RXP
SATA7TXN
SATA7TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

SATA 6G
SATA8RXN
SATA8RXP
SATA8TXN
SATA8TXP
SATA9RXN
SATA9RXP
SATA9TXN
SATA9TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

SATA 6G
SATA10RXN
SATA10RXP
SATA10TXN
SATA10TXP
SATA11RXN
SATA11RXP
SATA11TXN
SATA11TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

SATA 6G
SATA12RXN
SATA12RXP
SATA12TXN
SATA12TXP
SATA13RXN
SATA13RXP
SATA13TXN
SATA13TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

SATA 6G
SATA14RXN
SATA14RXP
SATA14TXN
SATA14TXP
SATA15RXN
SATA15RXP
SATA15TXN
SATA15TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

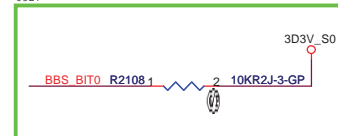
SATA 6G
SATA16RXN
SATA16RXP
SATA16TXN
SATA16TXP
SATA17RXN
SATA17RXP
SATA17TXN
SATA17TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

SATA 6G
SATA18RXN
SATA18RXP
SATA18TXN
SATA18TXP
SATA19RXN
SATA19RXP
SATA19TXN
SATA19TXP

Y7 >>> SATA_RXN4 56
Y5 >>> SATA_RXP4 56
AD3 >>> SATA_TXN4 56
AD1 >>> SATA_TXP4 56
Y3 >>> SATA_RXN5 57
Y1 >>> SATA_RXP5 57
AB3 >>> SATA_TXN5 57
AB1 >>> SATA_TXP5 57

0827



<Core Design>

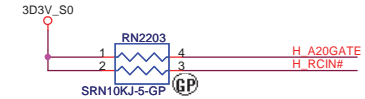
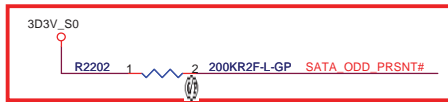
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Title			
PCH (SPI/RTC/LPC/SATA/IHDA)			
Size	Document Number	Rev	
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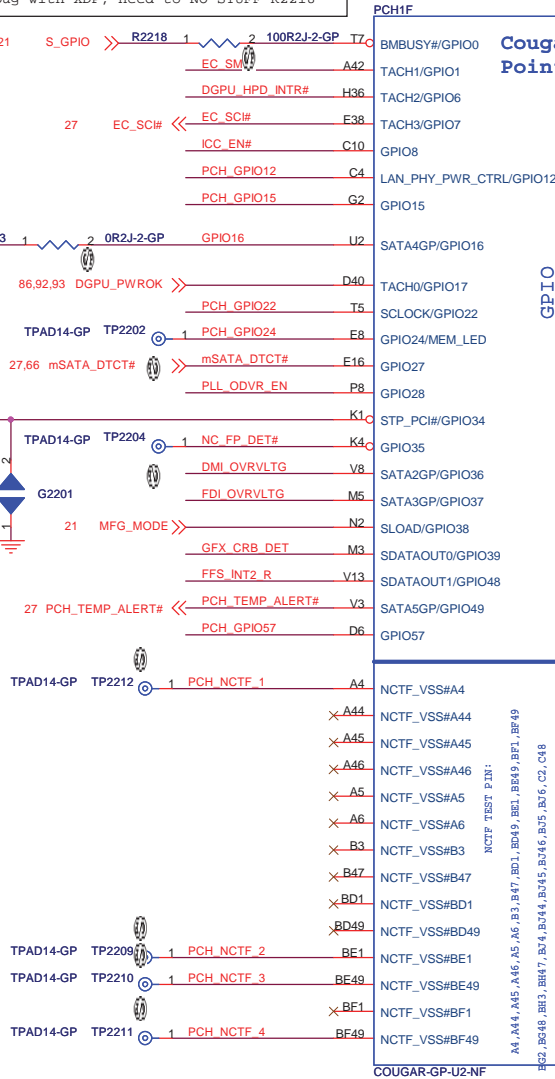
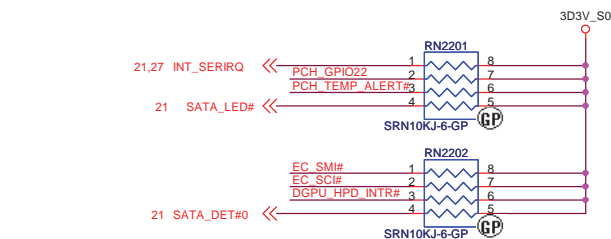
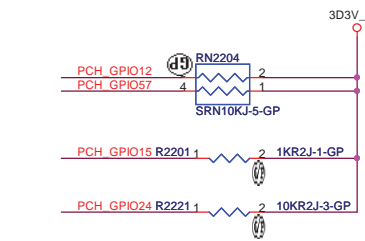
SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

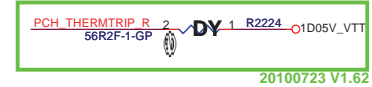
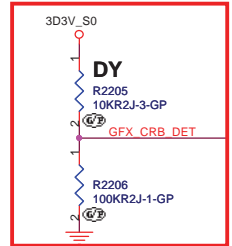
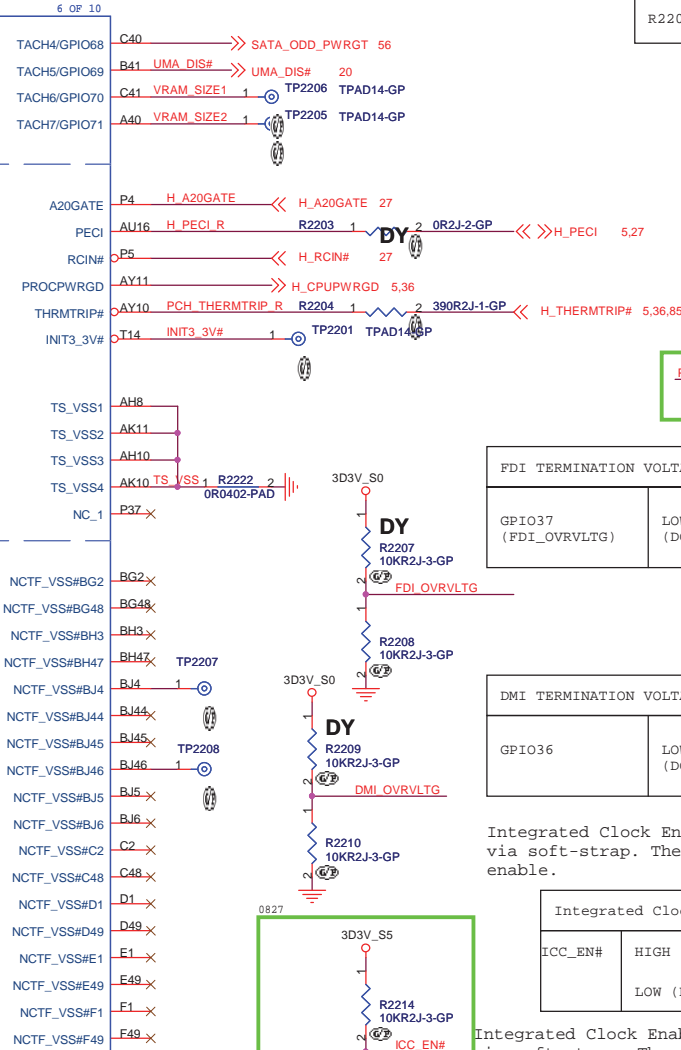


Cougar
Point

GPIO

NCTF

COUGAR-GP-U2-NF



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE	
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)	

<Core Design>	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH (GPIO/CPU)	
Size A3	Document Number LLW-1 / LGG-1
Date Tuesday, January 18, 2011	Sheet 22 of 94
Rev -1	

SSID = PCH

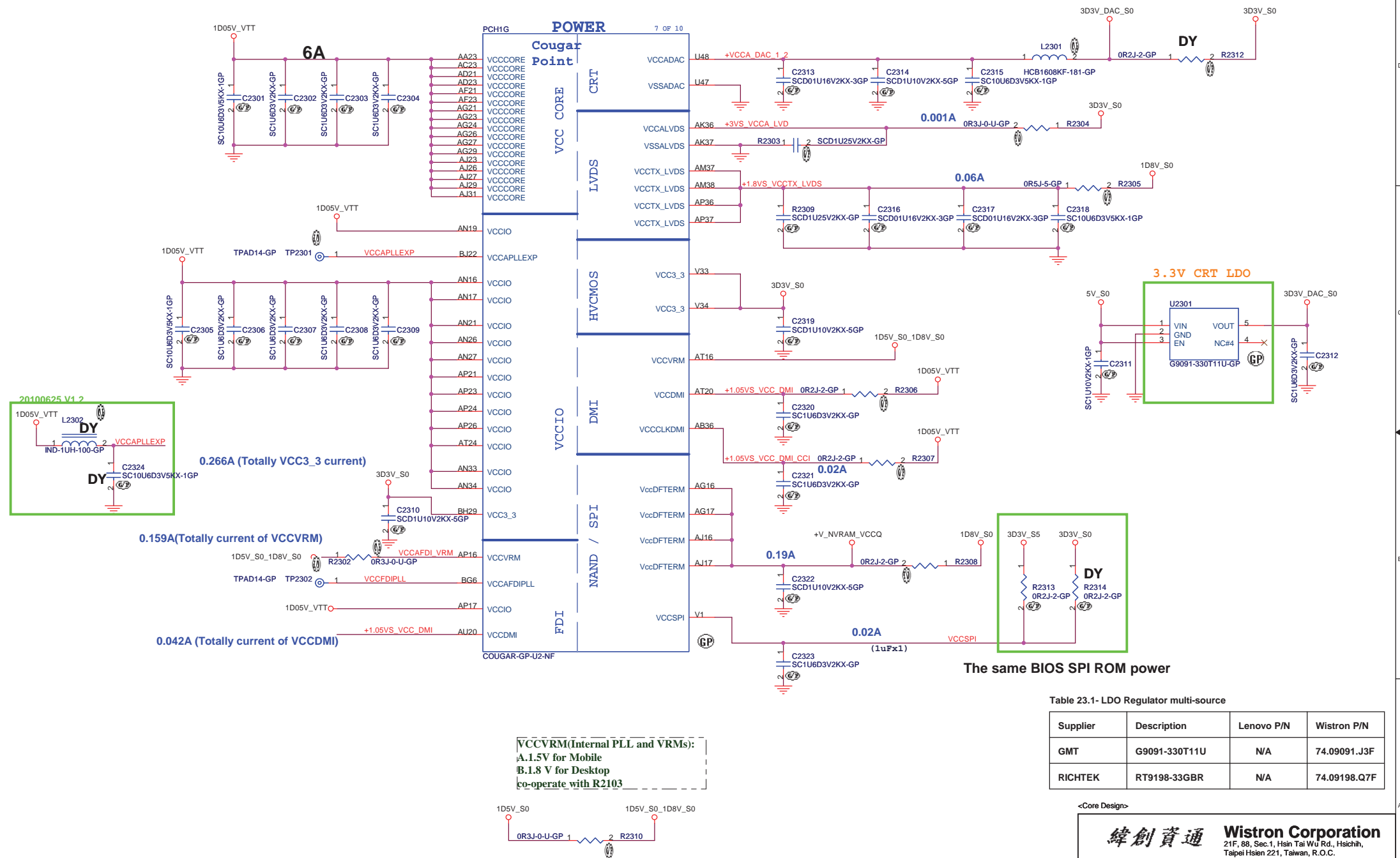


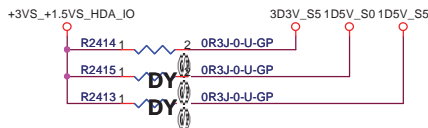
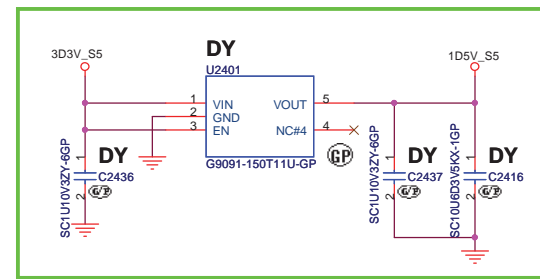
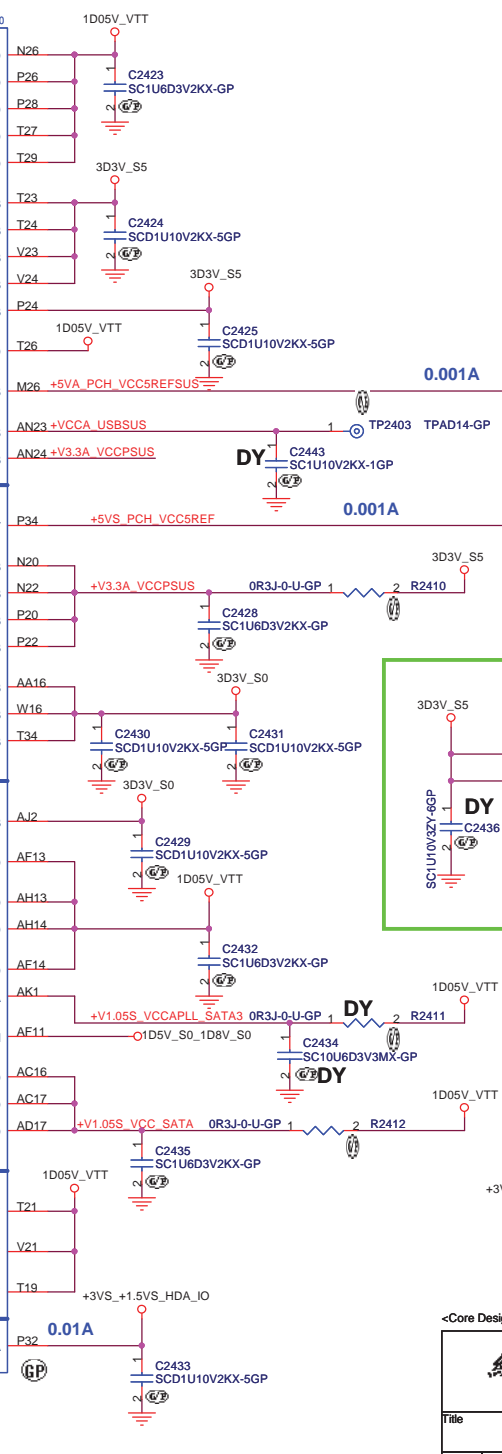
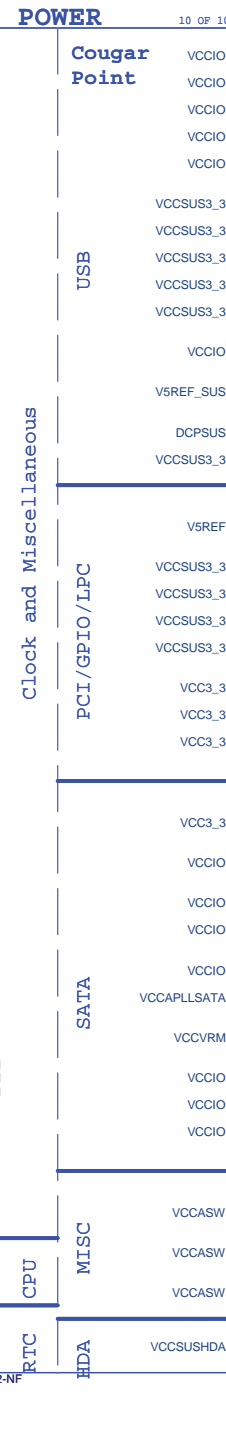
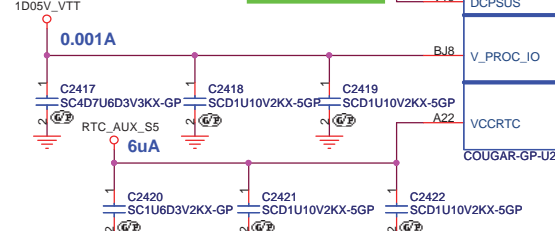
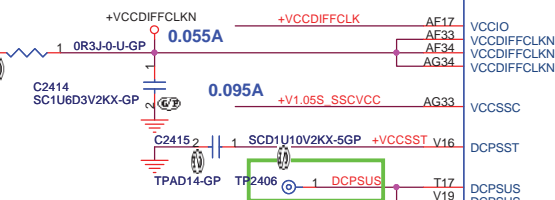
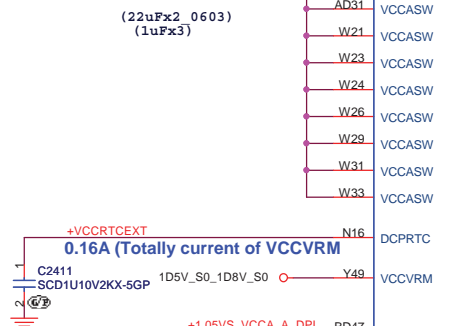
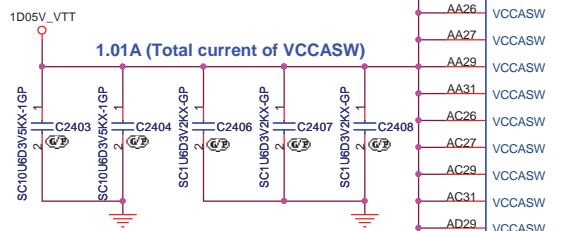
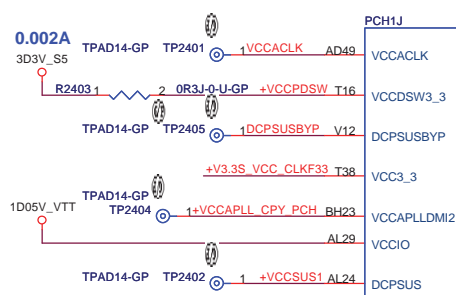
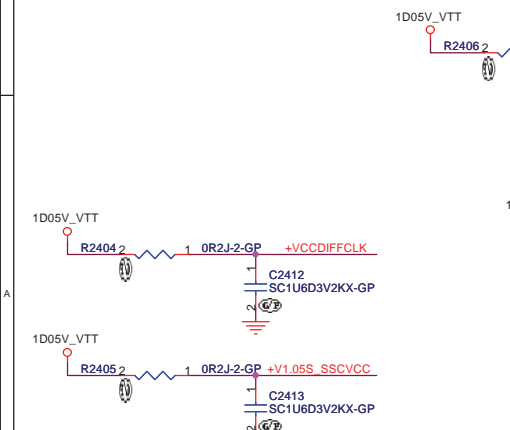
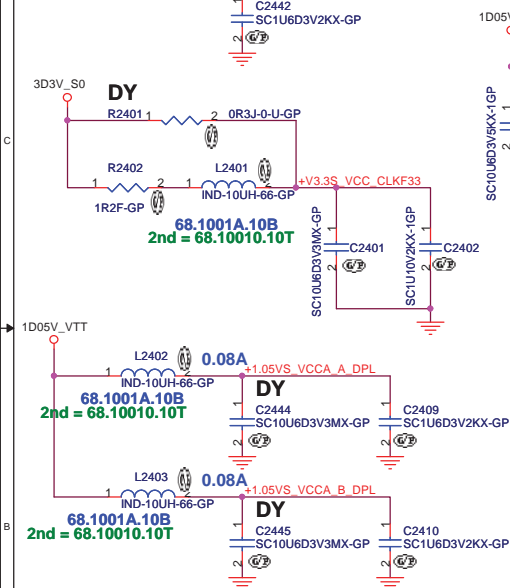
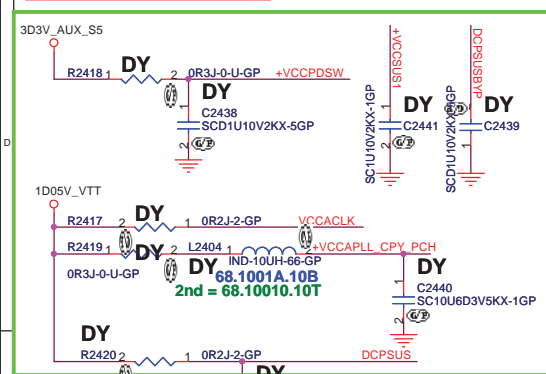
Table 23.1- LDO Regulator multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
GMT	G9091-330T11U	N/A	74.09091.J3F
RICHTEK	RT9198-33GBR	N/A	74.09198.Q7F

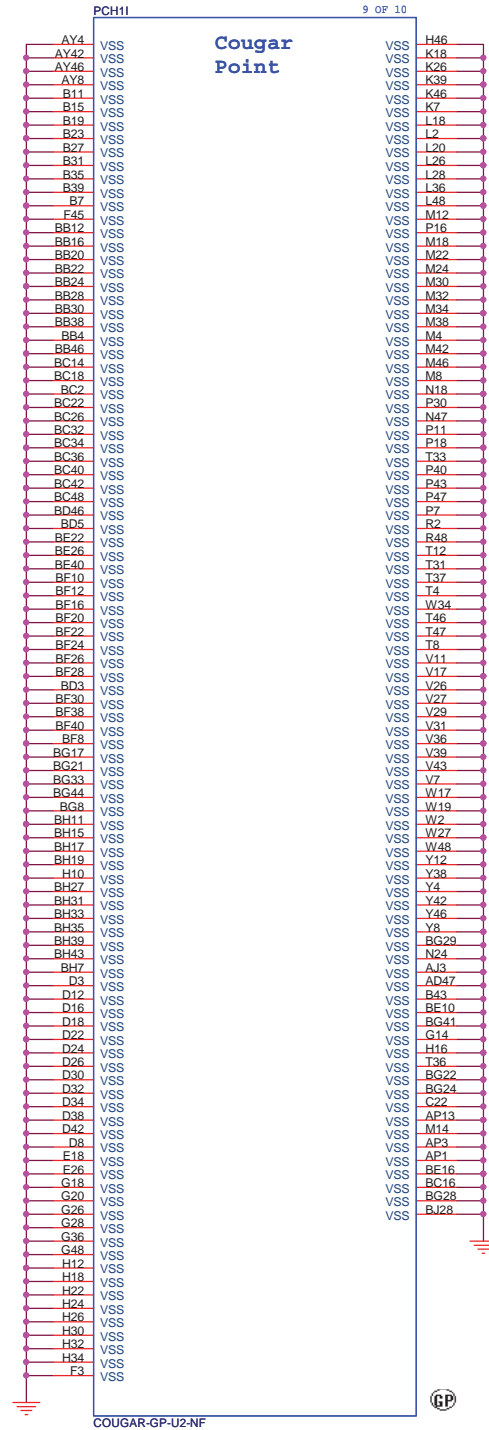
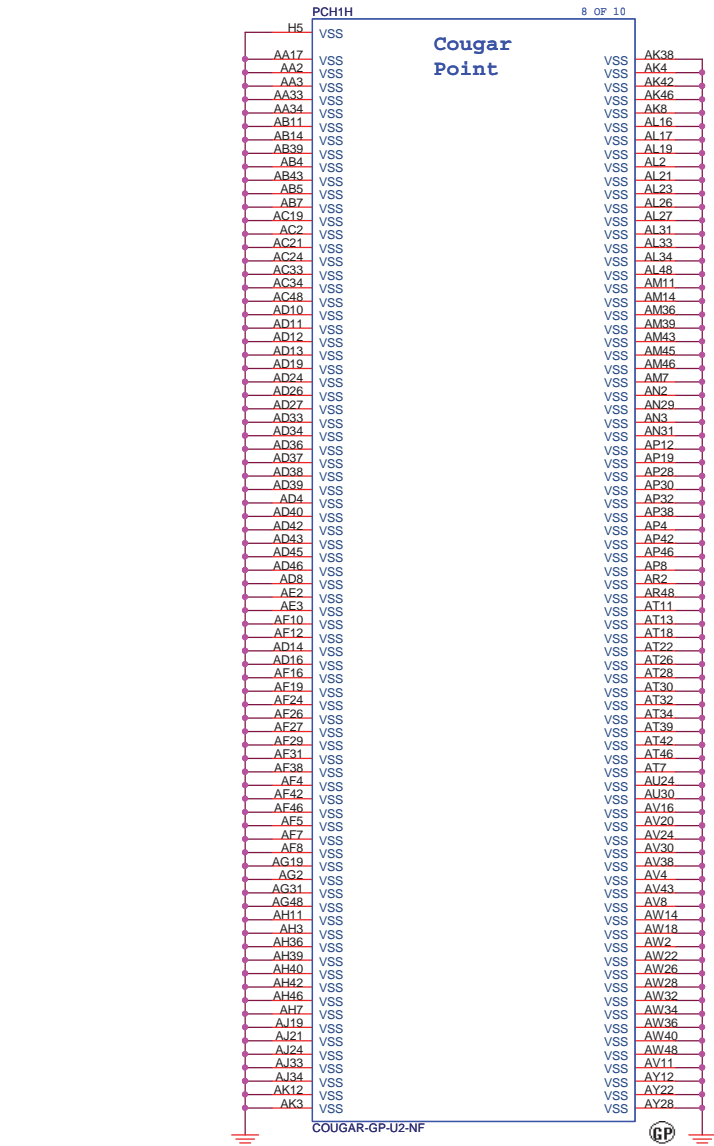
<Core Design>

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Title		
PCH (POWER1)		
Size A3	Document Number	Rev
	LLW-1 / LGG-1	-1
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SSID = PCH



SSID = PCH



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Title		PCH (VSS)	
Size	Document Number	Rev	
A3	LLW-1 / LGG-1	-1	
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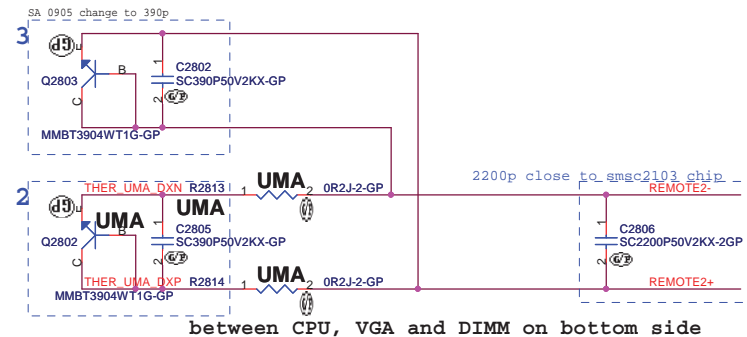
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		Sheet 26 of 94



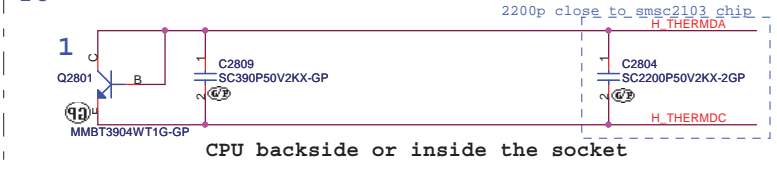
SSID = Thermal

Thermal sensor

Close to SO-DIMM side.



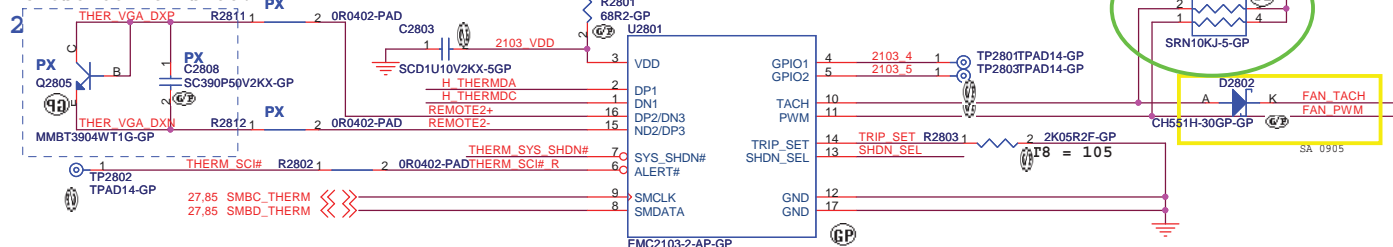
T8



CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

Close to VGA side. PX



pin6, ALERT# OD
pin7, SYS_SHDN# OD

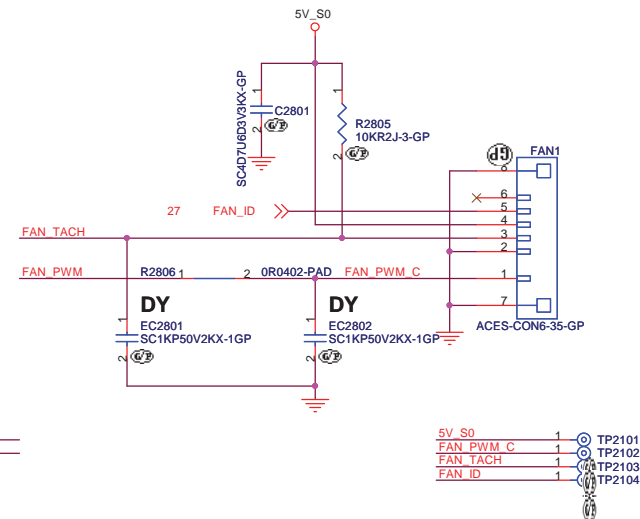
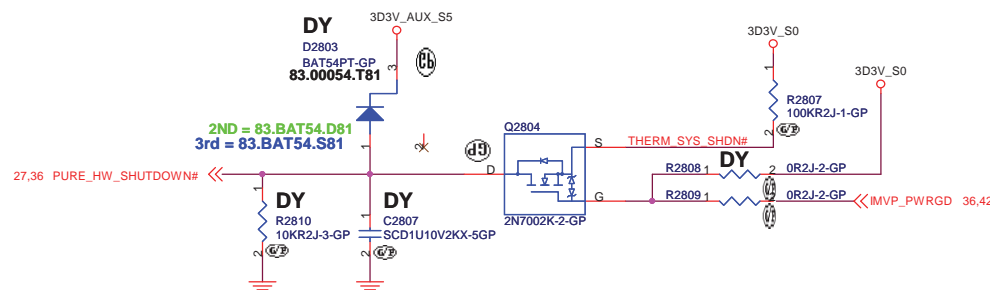


Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11
CHENMKO	CH3904WGP	N/A	84.03904.Y11

Table 28.2- Surface Mount Schottky Barrier

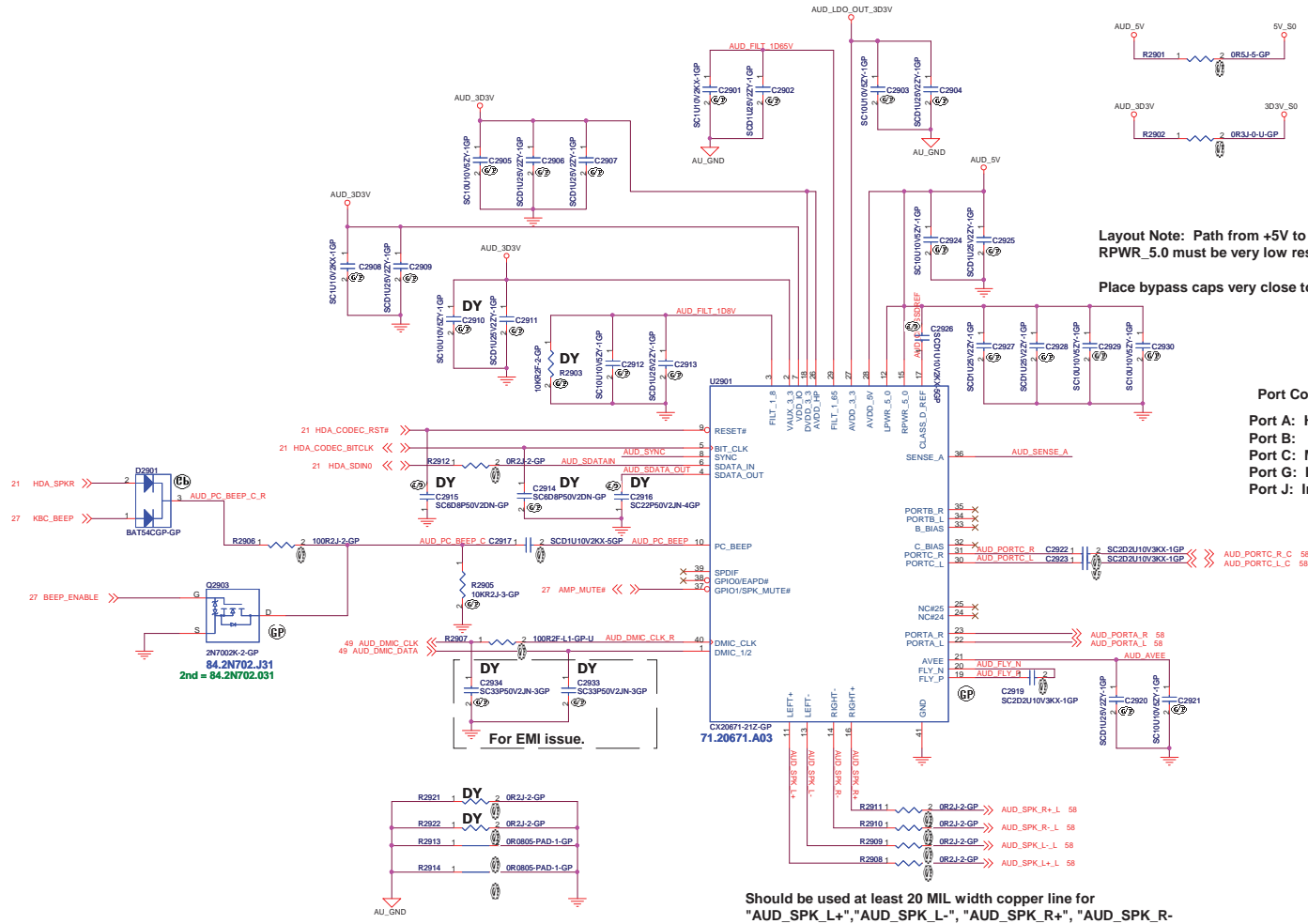
Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	BAT54PT	N/A	83.00054.T81
PANJIT	BAT54	N/A	83.BAT54.D81
Power Silicon Inc.	BAT54C	N/A	83.BAT54.S81

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Title	Document Number	Rev
THERMAL SENSOR SMSC EMC2103	LLW-1 / LGG-1	-1
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AUDIO CODEC



Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

Port Configuration

Port A: Headphone jack

Port B:

Port C: Microphone jack

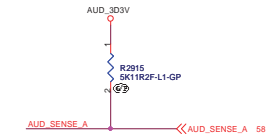
Port G: Internal stereo speakers

Port J: Internal stereo digital mic

JACK DETECT RESISTORS

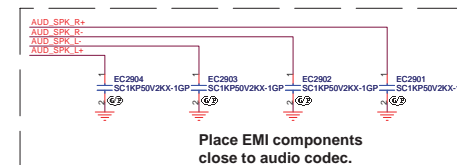
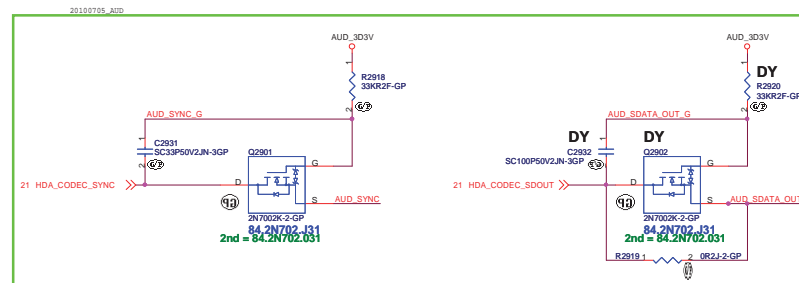
Close to Pin36

SENSE PIN A



Should be used at least 20 MIL width copper line for
"AUD_SPK_L+", "AUD_SPK_L-", "AUD_SPK_R+", "AUD_SPK_R-

Place R2913/R2914 under CODEC,
and place R2921/R2922 near CODEC



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Title

AMP

Size

Document Number

Rev

A3

LLW-1 / LGG-1

-1

Date:

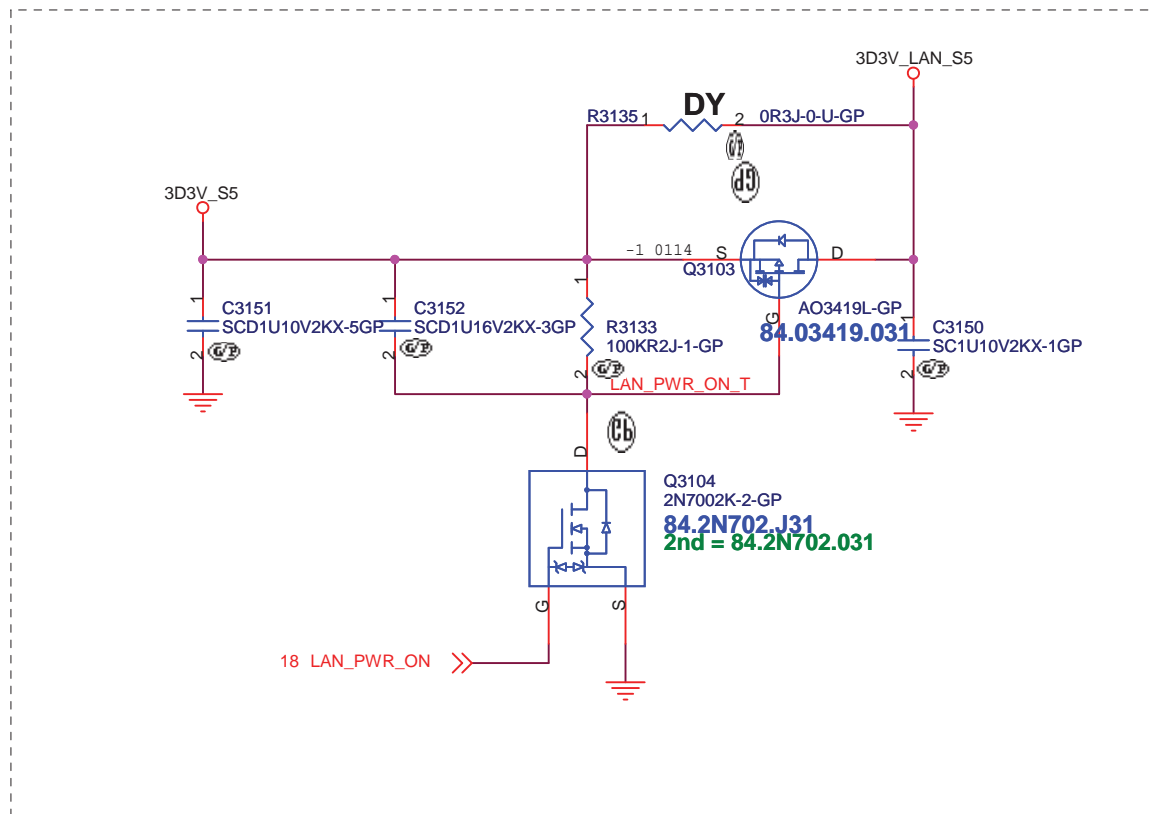
Tuesday, January 18, 2011

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Title

LAN PWR SW

Size
A4

Document Number

LLW-1 / LGG-1

Rev
-1

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Title			
1394			
Size A4	Document Number LLW-1 / LGG-1		Rev -1
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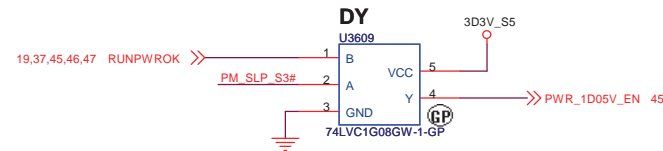
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title					
Smart Card Reader					
Size	Document Number		Rev		
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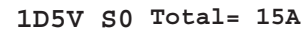
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Title		USB3.0	
Size	Document Number		Rev
A4	LLW-1 / LGG-1		-1
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Power Sequence

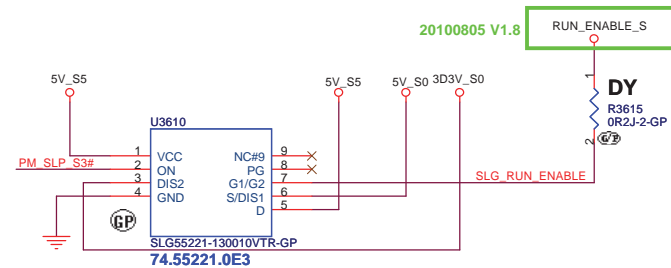


Run Power



MAX Current 3000 mA

Design Current 2100 mA



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Title

POWER SEQUENCE

Size

Document Number

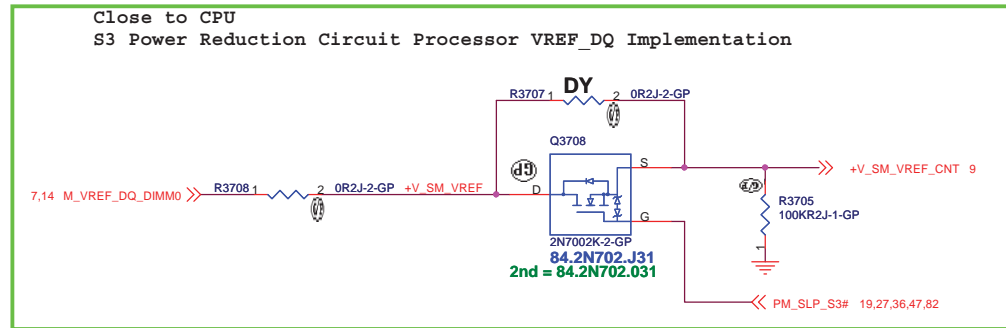
LLW-1 / LGG-1

Rev

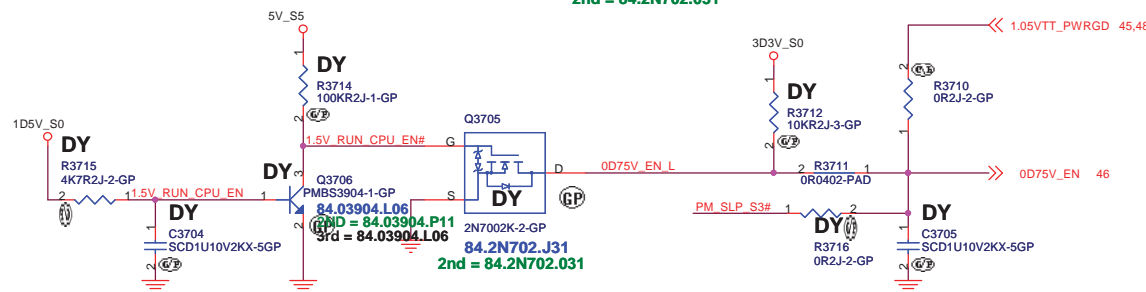
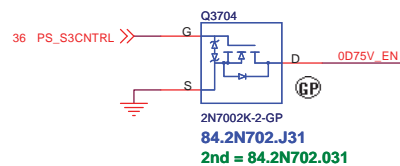
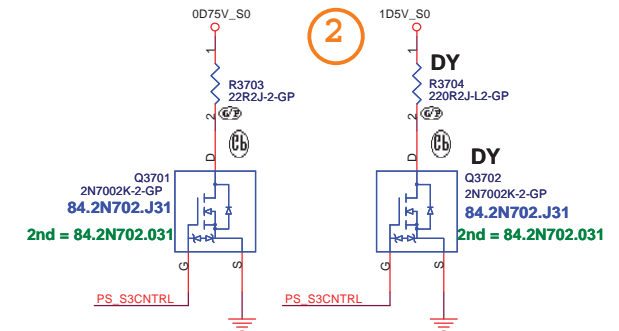
Date: Tuesday, January 18, 2011

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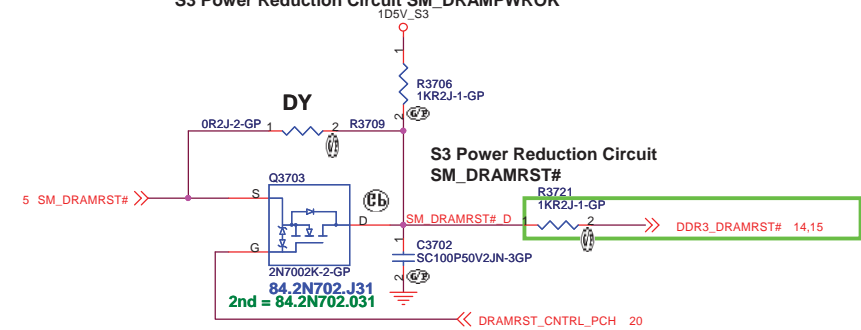
94



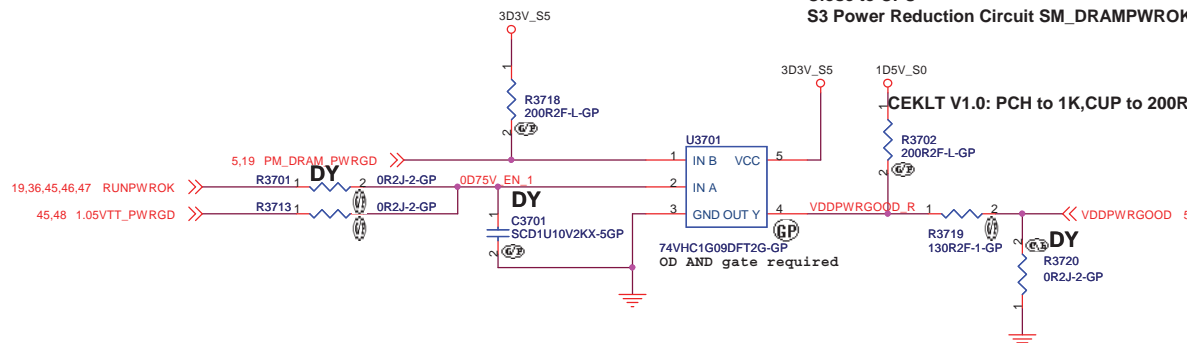
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

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Title		
ADAPTER OCP / S3 reduction		
Size A3	Document Number	Rev -1
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<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
TitleDCIN_JACK		
Size	Document NumberLLW-1 / LGG-1	Rev-1
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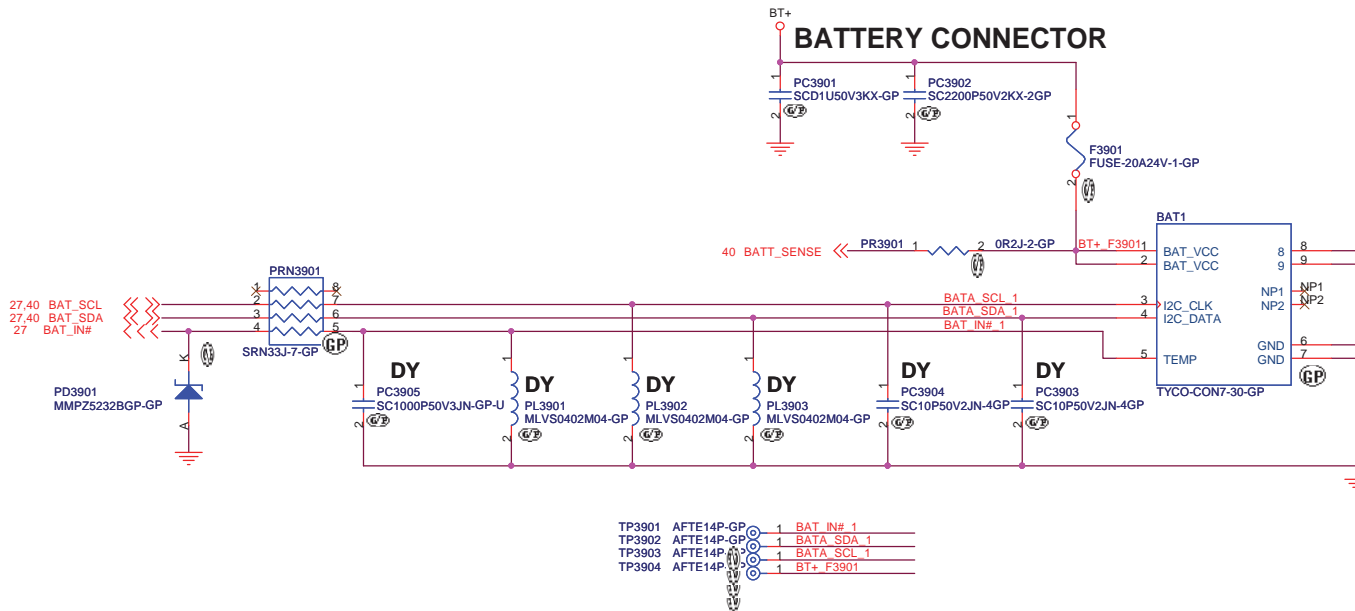


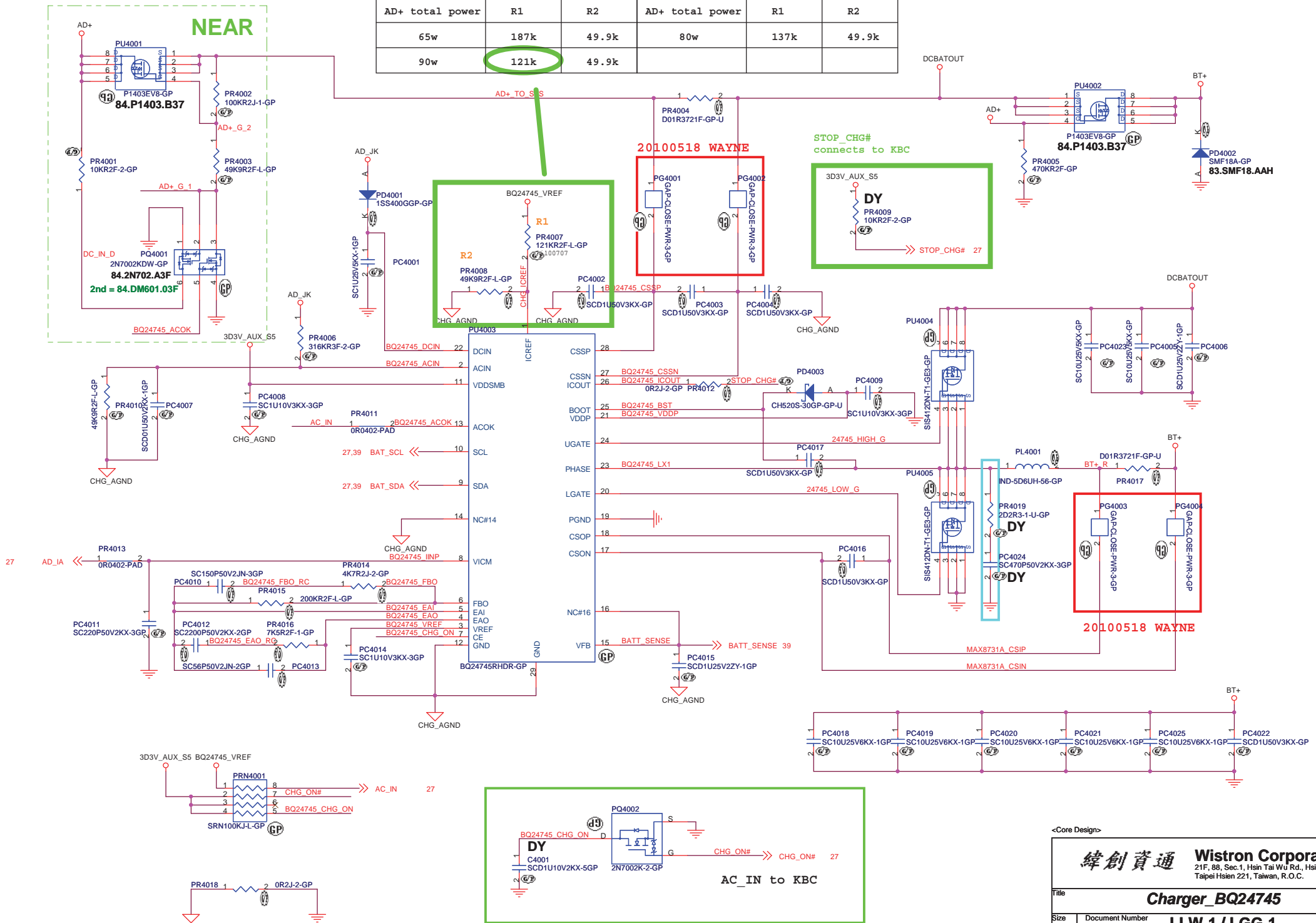
Table 39.1- Surface Mount Zener ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	MMPZ5232BGP	N/A	83.5R603.R3F
DIODES	MMSZ5232BS-7-F	N/A	83.5R603.K3F
PANJIT	MMSZ5232BS	N/A	83.5R603.Q3F

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Title BATT_CONN	
Size	Document Number LLW-1 / LGG-1
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AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



```
SSID = PWR.Plane.Regulator_5v3p3v
```

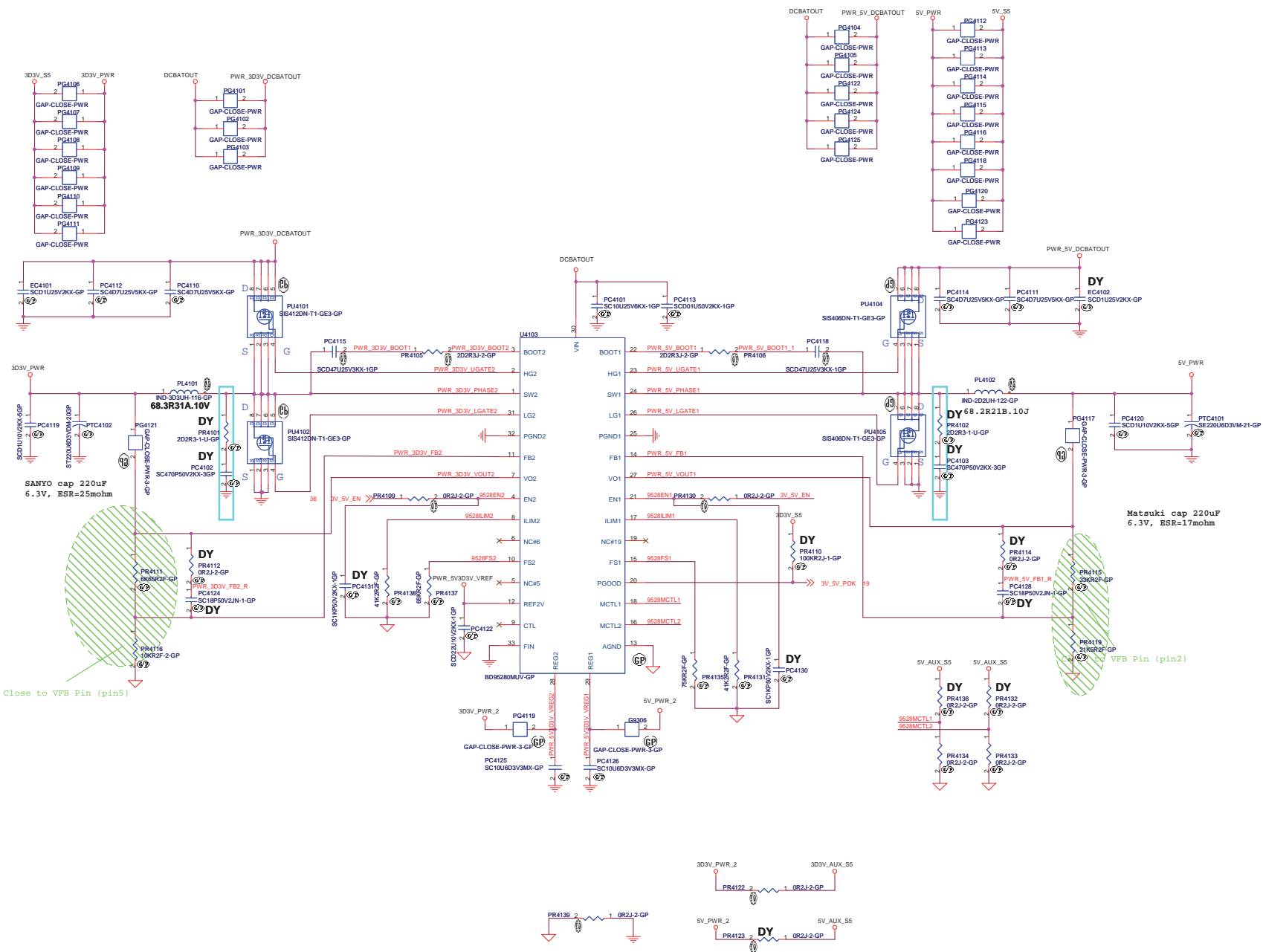


Table 41.1 - POSCAP multi-source

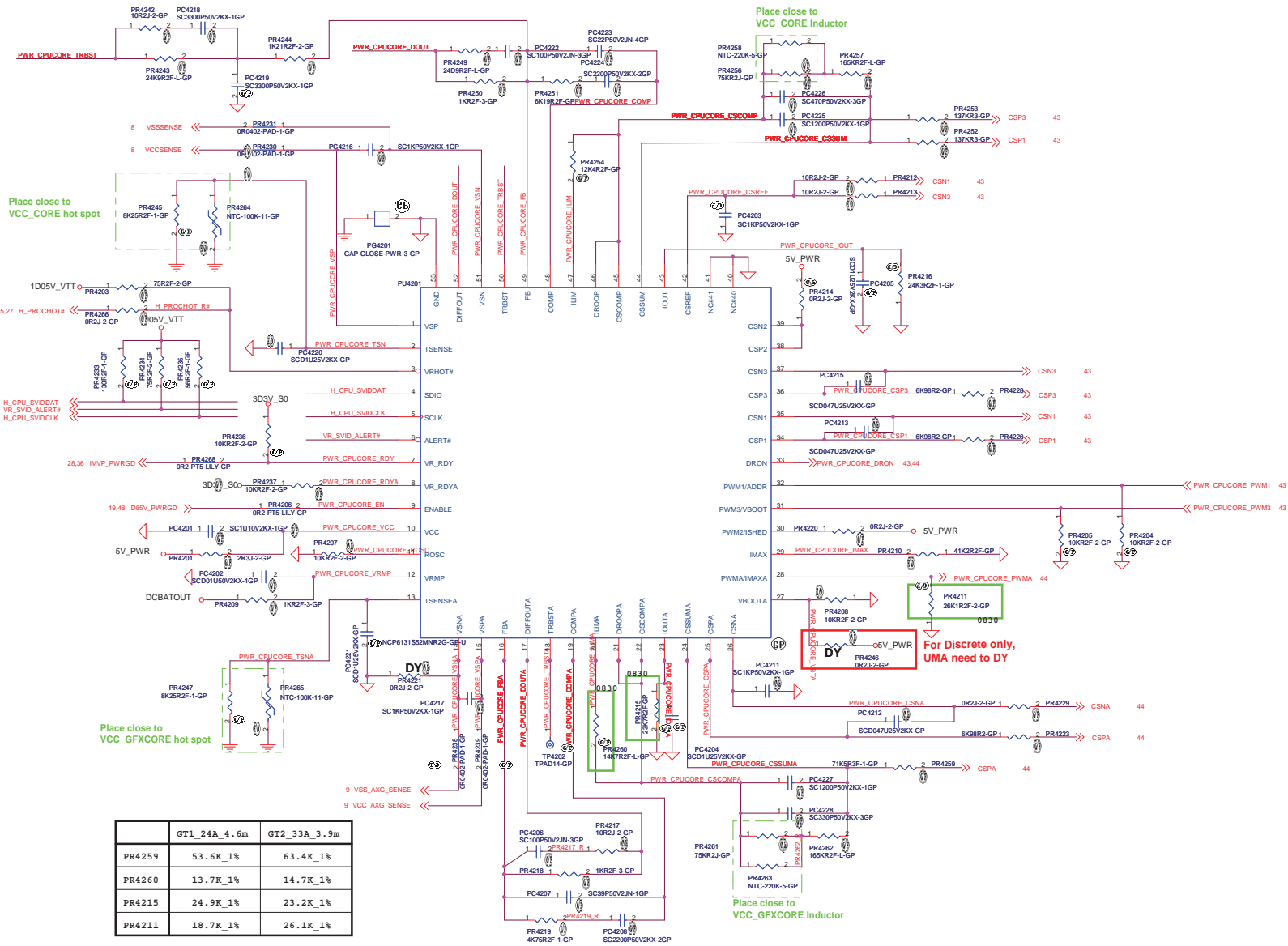
Supplier	Description	Lenovo P/N	Wistron P/N
SANYO	6TPE220MAP	N/A	77.22271.27L
NEC-TOKIN	V0J227M(25)12RE	N/A	77.C2271.00L

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Title			
DC/DC 3D3V5V			
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WWW.AliSaler.Com



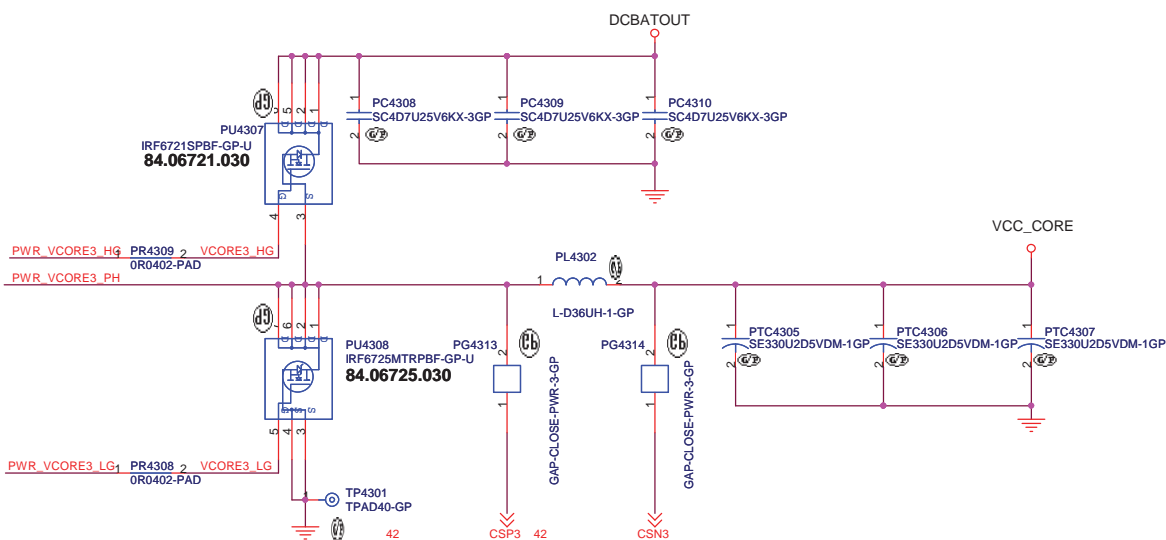
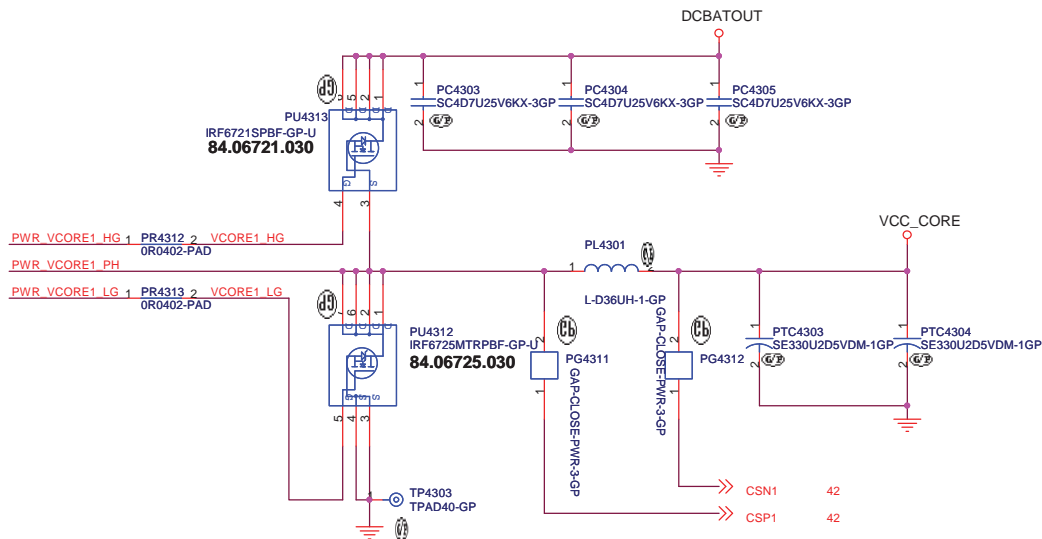
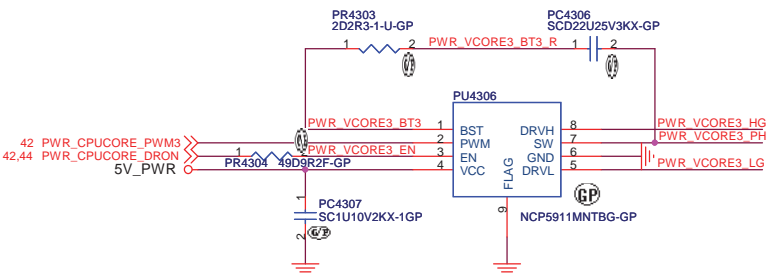
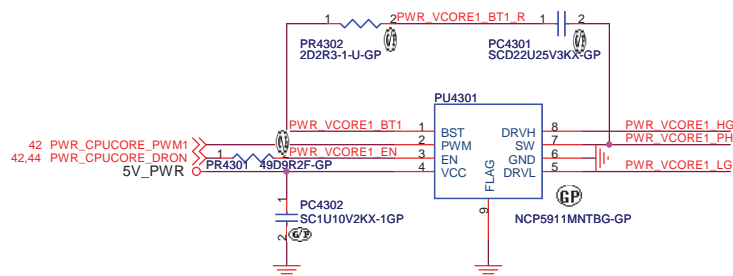
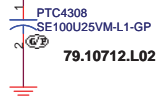
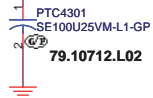
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Title DC/DC CPU CORE1_NCP6131
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DCBATOUT

DCBATOUT

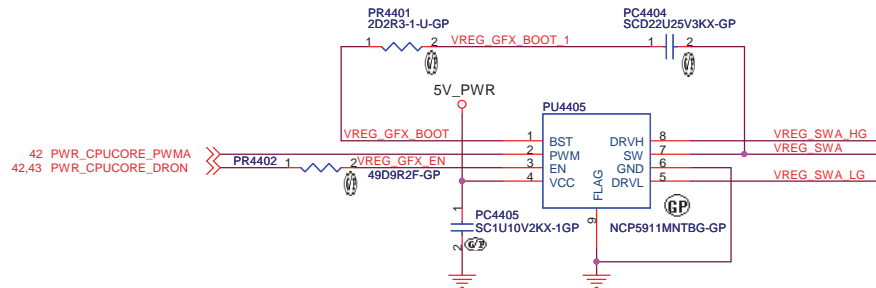
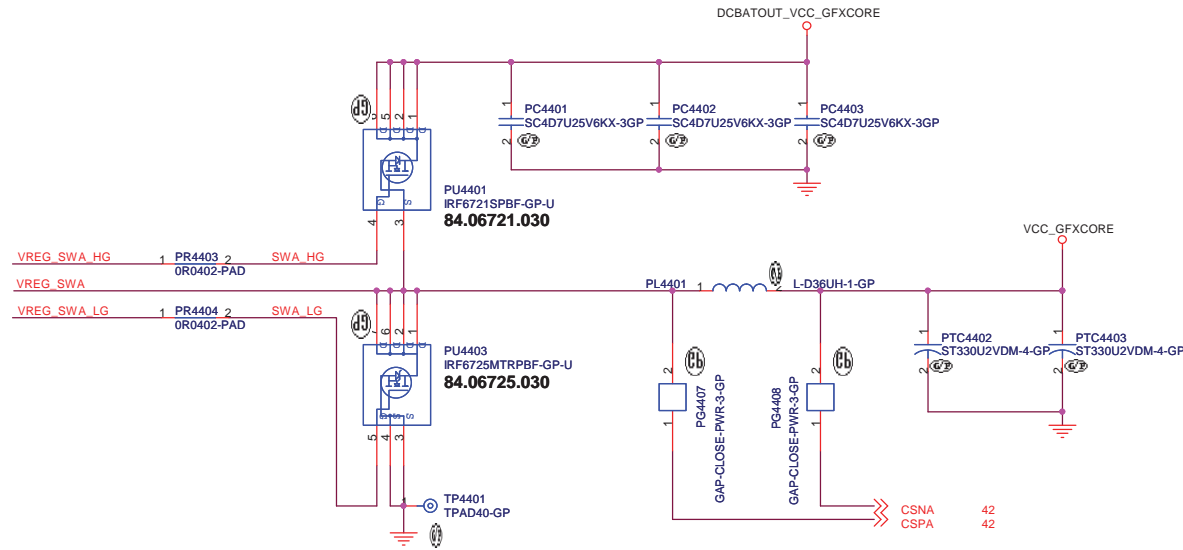
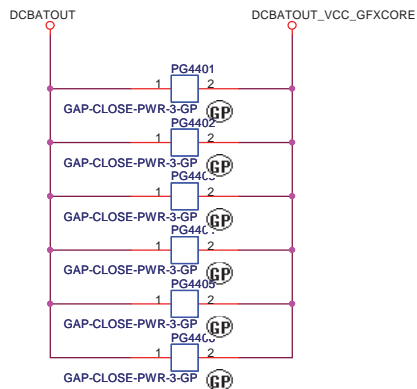


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Taipei Hsien 221, Taiwan, R.O.C.

Title DC/DC CPU CORE2_NCP6131
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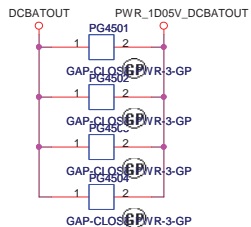
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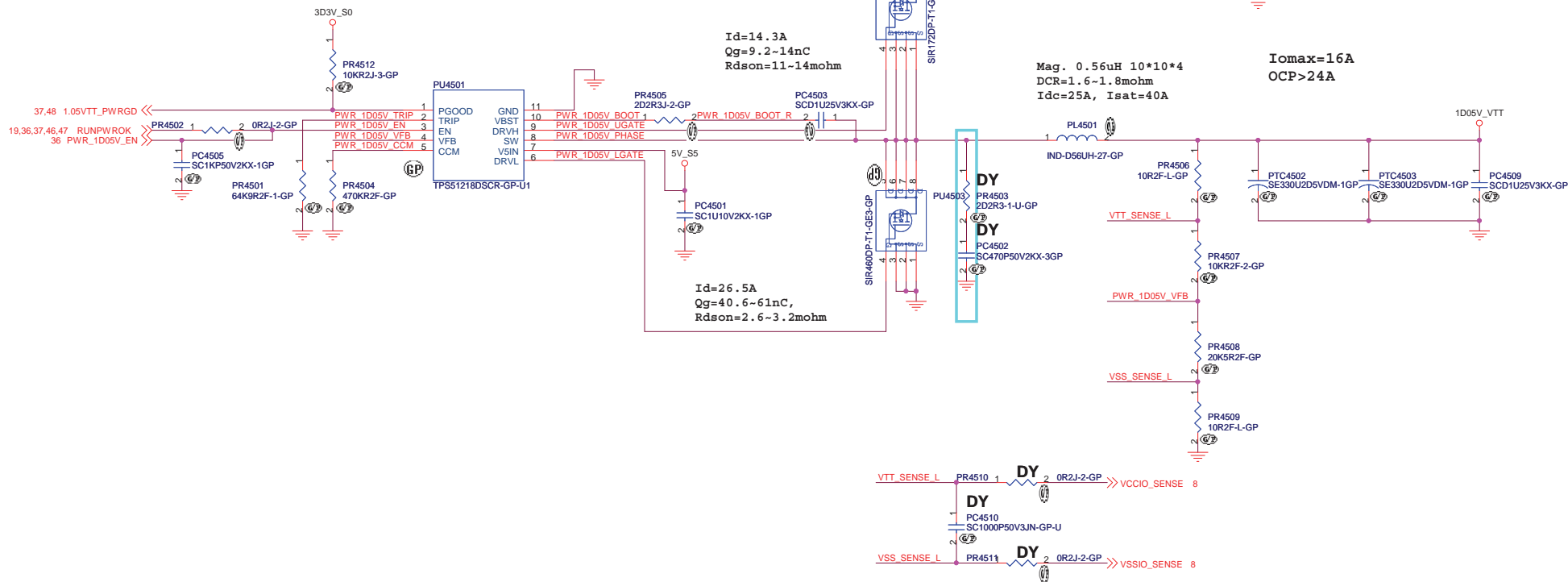
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Title			DC/DC CPU CORE3_NCP6131
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TPS51218 for 1D05V

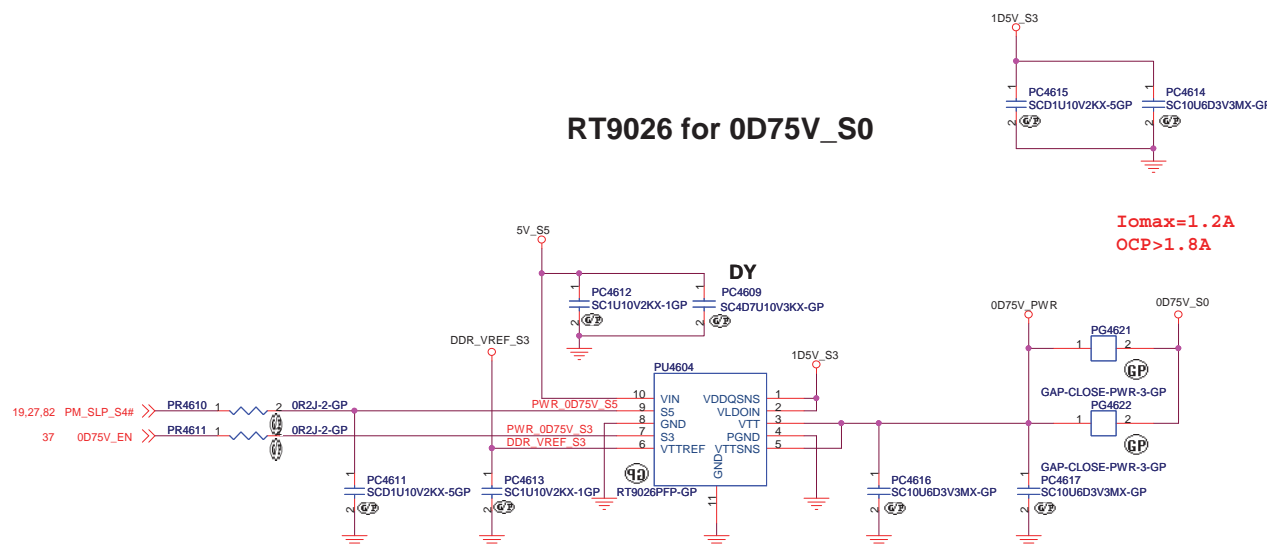
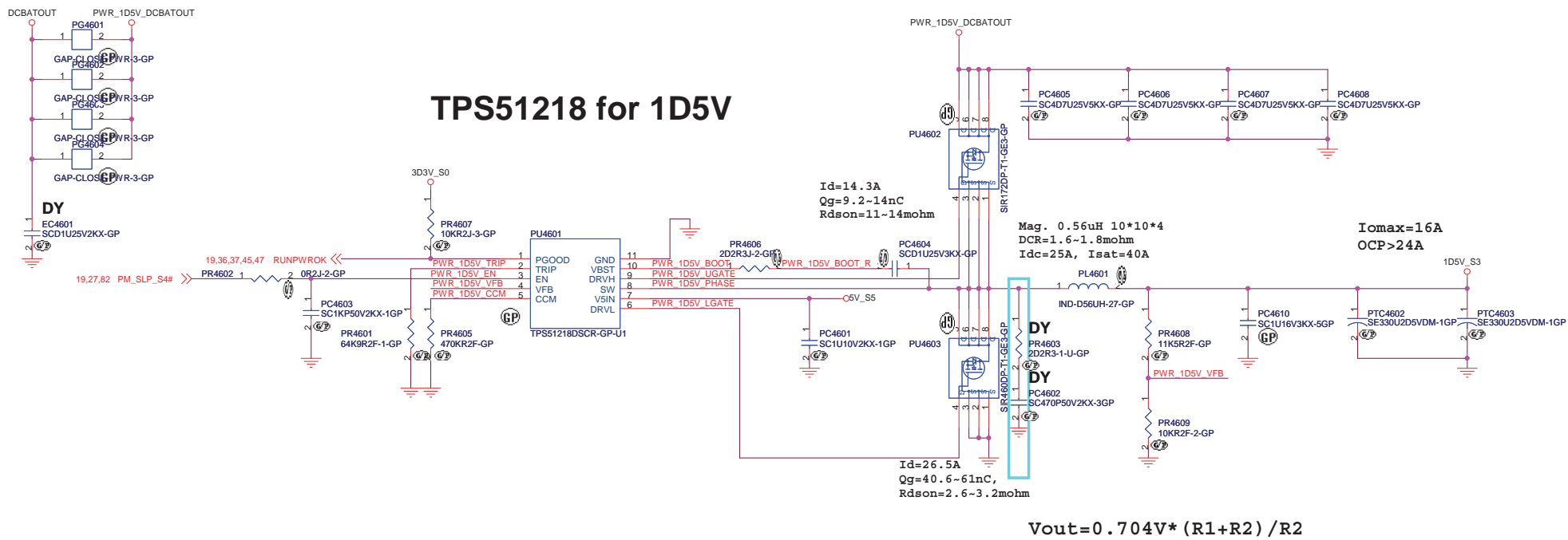


$$V_{out}=0.704V \cdot (R1+R2) / R2$$

<Core Design>

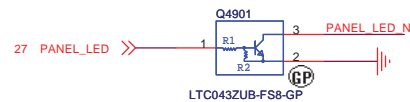
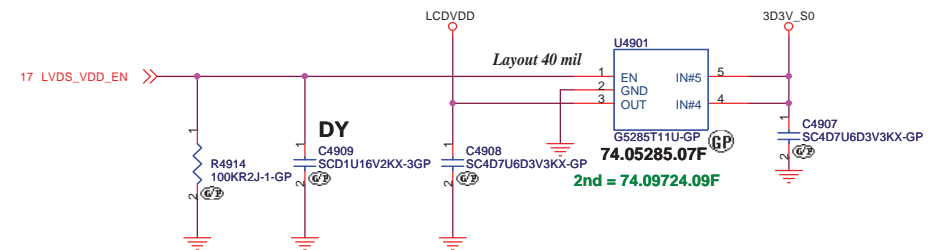
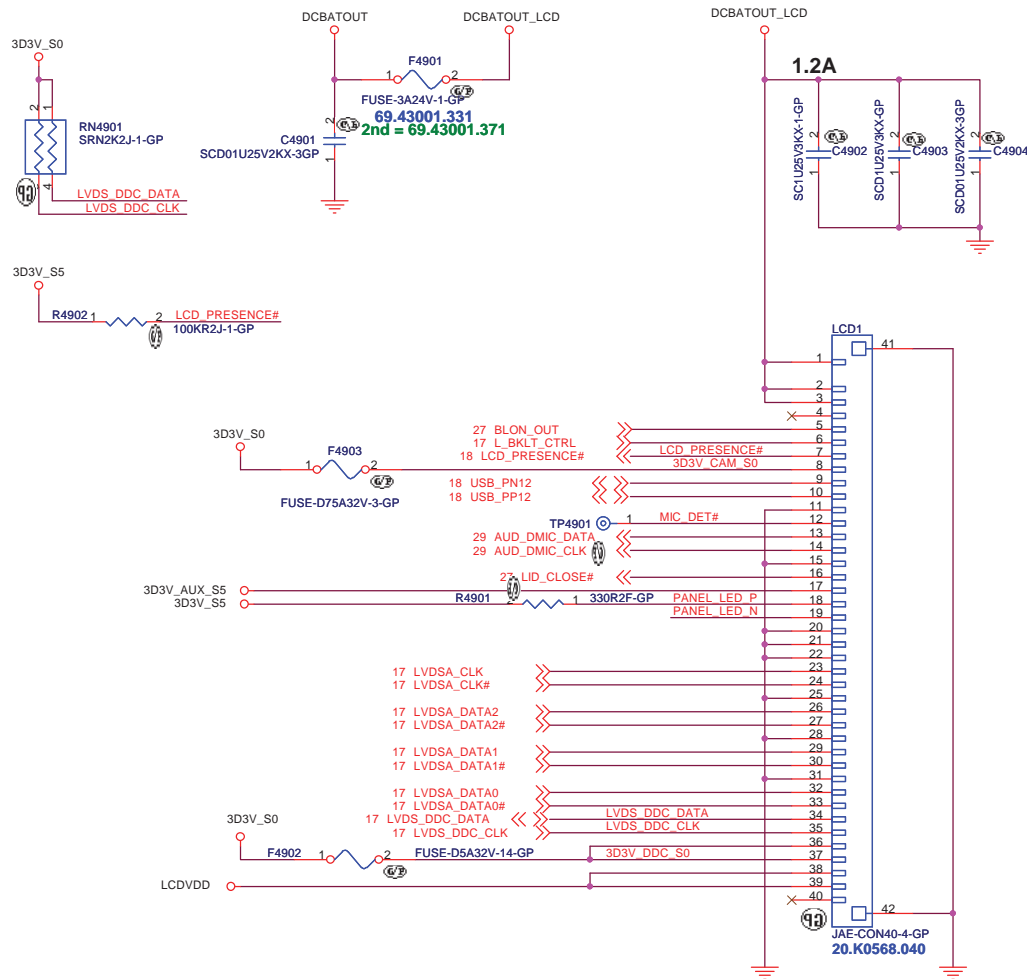
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Title		TPS51218_1D05V	
Size	Document Number	LLW-1 / LGG-1	Rev
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LCD / Inverter Connector



Near LCD1

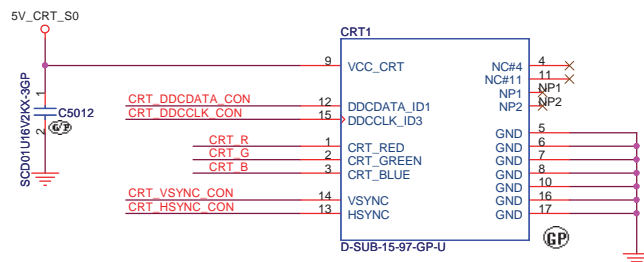
LID_CLOSE#	1	AFTP4901	AFTE14P-GP
AUD_DMIC_CLK	1	AFTP4902	AFTE14P-GP
AUD_DMIC_DATA	1	AFTP4903	AFTE14P-GP
3D3V_DDC_S0	1	AFTP4904	AFTE14P-GP

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Title			
LCD CONNECTOR			
Size A3	Document Number LLW-1 / LGG-1		Rev -1
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CRT CONNECTOR

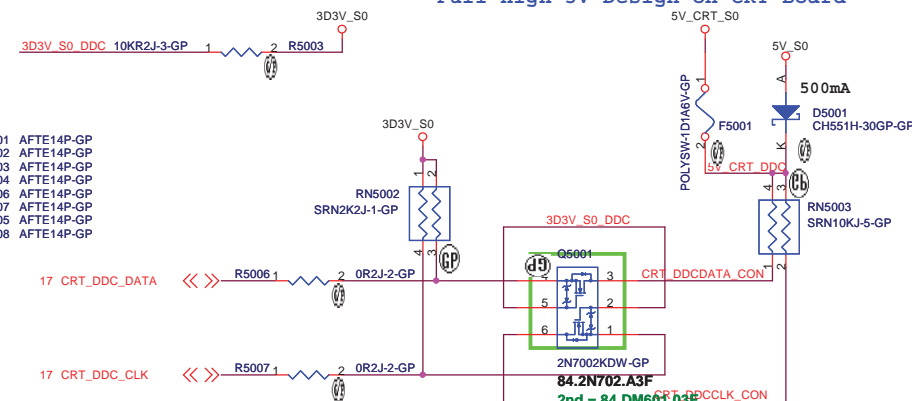


Near CRT1

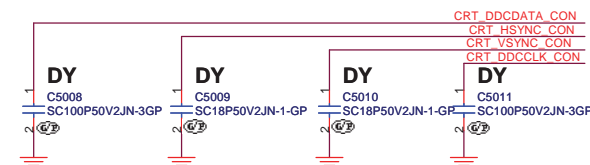
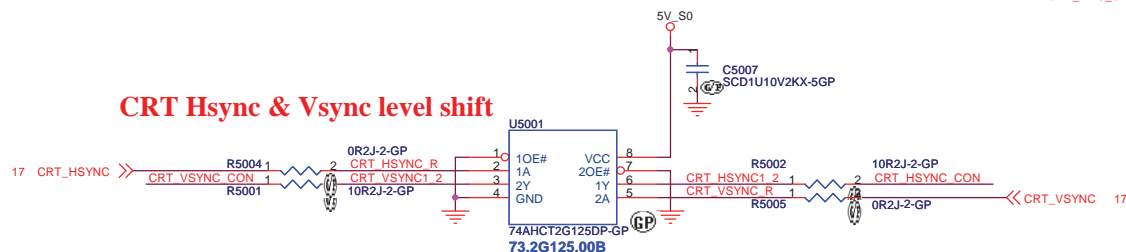


CRT DDCDATA & DDCCLK level shift

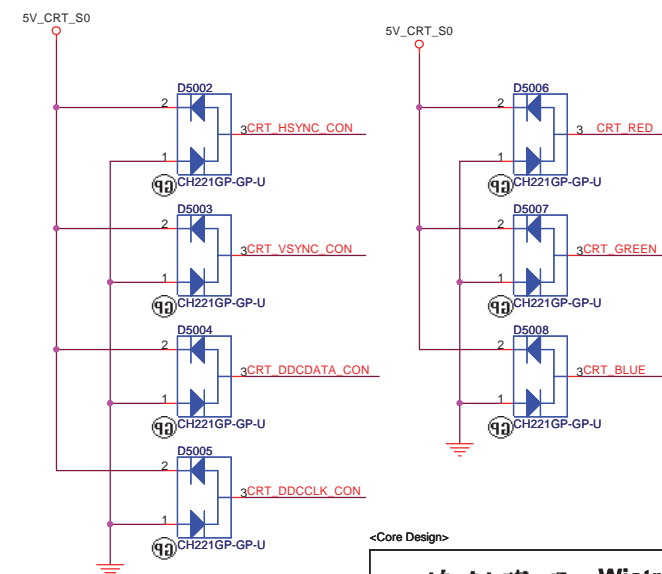
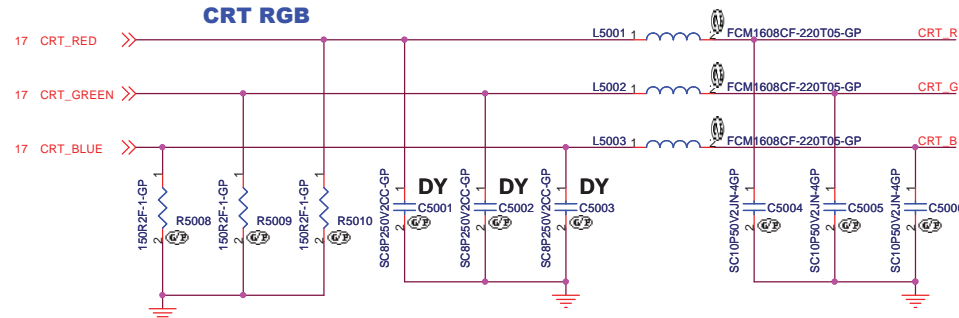
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift



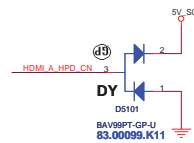
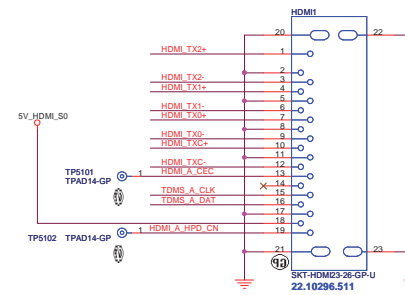
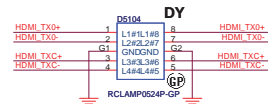
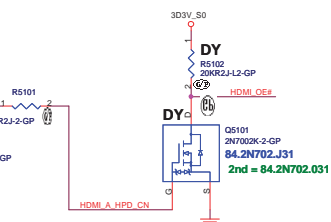
CRT RGB



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector		
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HDMI DATA2+_R SRN0J-6-GP 2 4

HDMI DATA2+_R SRN0J-6-GP 1 4

HDMI DATA1+_R SRN0J-6-GP 2 4

HDMI DATA1+_R SRN0J-6-GP 1 4

HDMI DATA0+_R SRN0J-6-GP 2 4

HDMI DATA0+_R SRN0J-6-GP 1 4

HDMI_CLK+_R SRN0J-6-GP 2 4

HDMI_CLK+_R SRN0J-6-GP 1 4

RN5103

RN5104

RN5106

RN5107

HDMI_TX2+

HDMI_TX2-

HDMI_TX1+

HDMI_TX1-

HDMI_TX0+

HDMI_TX0-

HDMI_TXC+

HDMI_TXC-

RN5101

RN5102

RN5103

RN5104

RN5105

RN5106

RN5107

RN5108

RN5109

RN5110

RN5111

RN5112

RN5113

RN5114

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Pin configuration diagram for the 2N7002N GP MOSFET. The gate is connected to 303V_S0. The drain is connected to PCH_HDMI_DATA. The source is connected to PCH_HDMI_CLK. The MOSFET is labeled 2N7002N GP, 84.2N702.A3F, and 2nd = 84.DM601.03F.

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DISPLAY PORT CONNECTOR

Size
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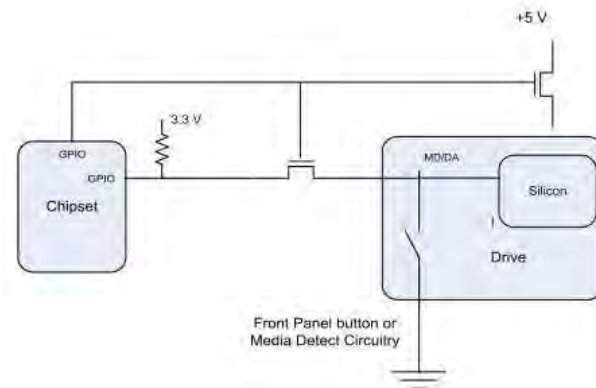
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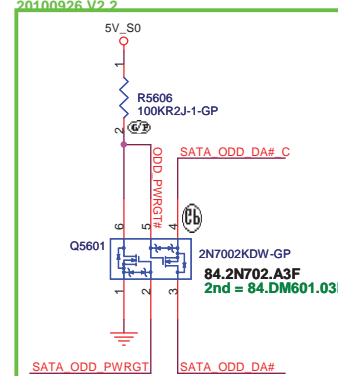
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ODD Connector



SUPPORT ZERO SATA ODD



SATA ODD_PWRGT 4
SATA ODD_BA# 3

RN5601 1
2

SRN10KJ-5-GP 4 3

3D3V_S0

0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD

ESATA Connector

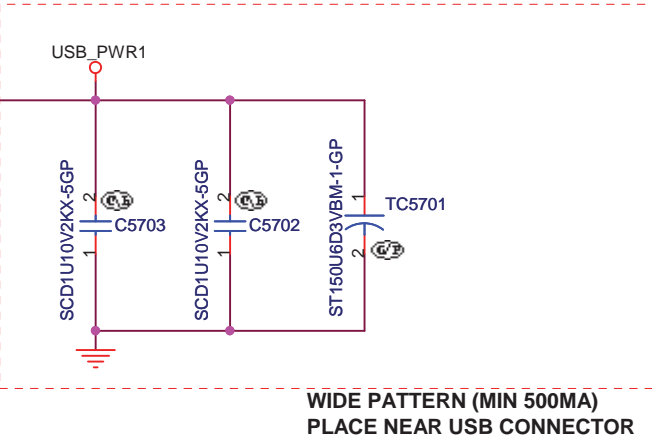
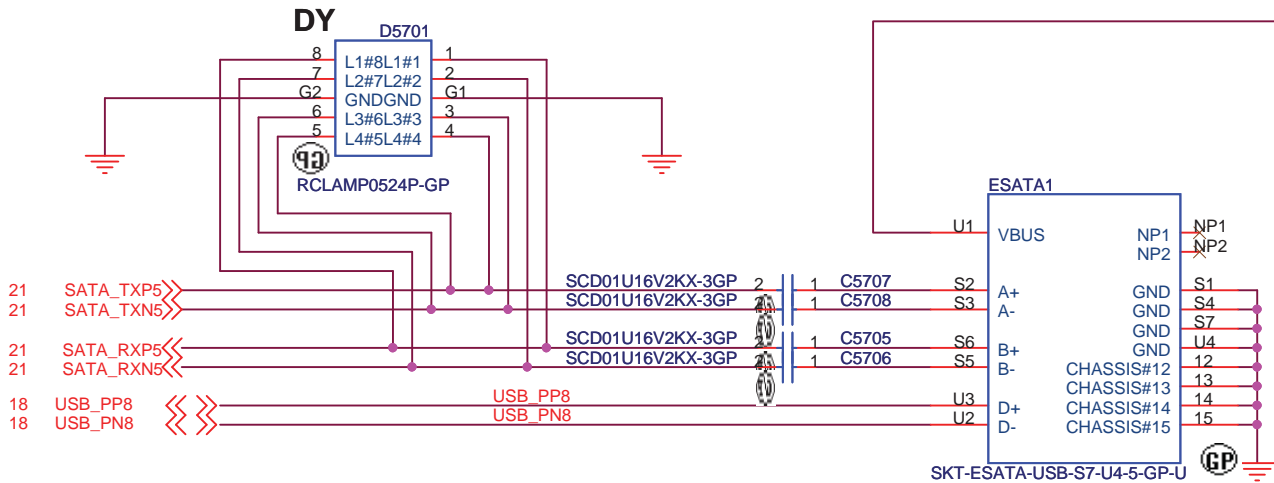
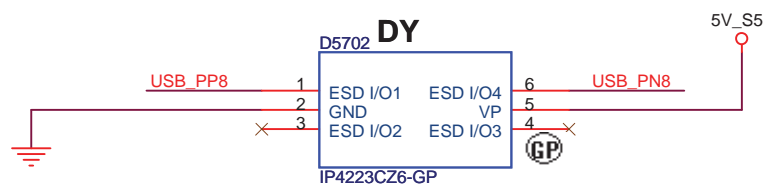
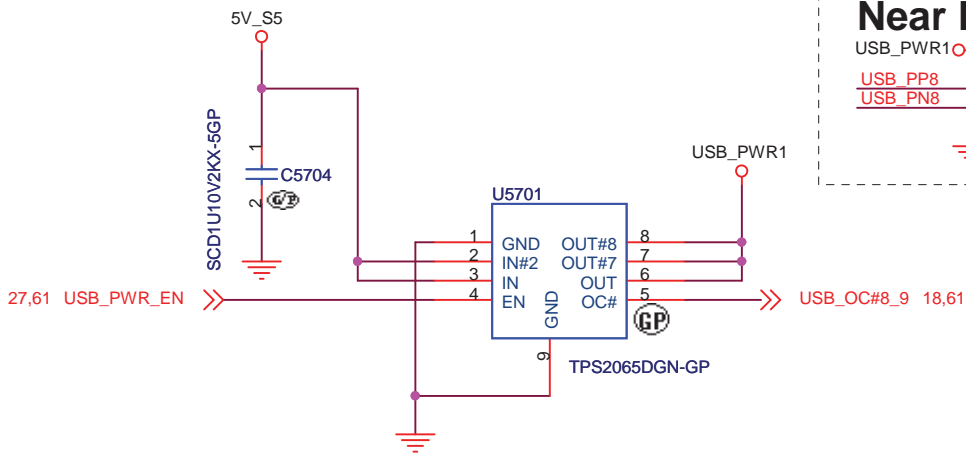
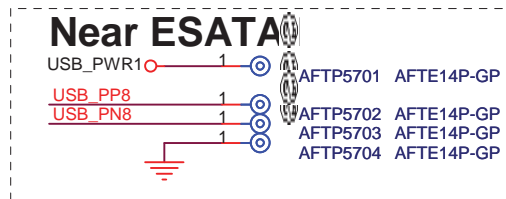


Table 57.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2065DGN4	54Y9024BA	74.02065.079
ROHM	BD8012FVJ	54Y9024AA	74.08012.07G

Table 57.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L



<Core Design>

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Title

ESATA CONNECTOR

Size A4

Document Number

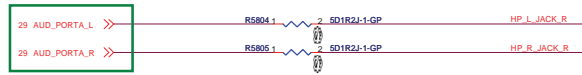
Rev -1

LLW-1 / LGG-1

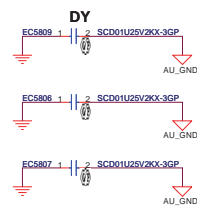
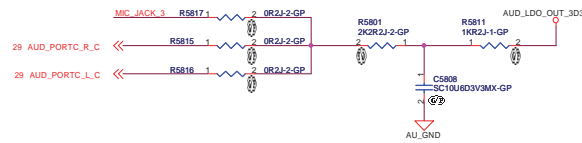
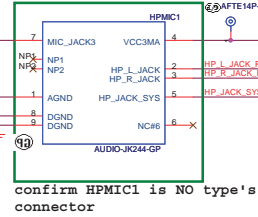
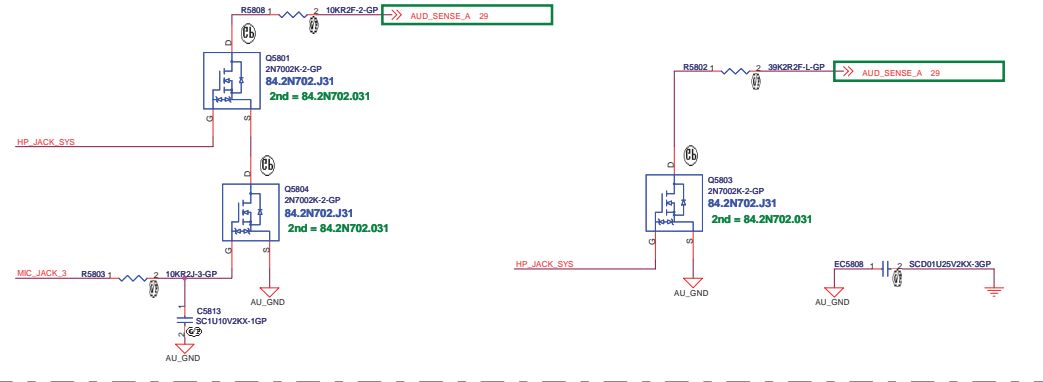
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NEAR HEADPHONE CONN



JACK SENSE



INTERNAL STEREO SPEAKERS

Port G

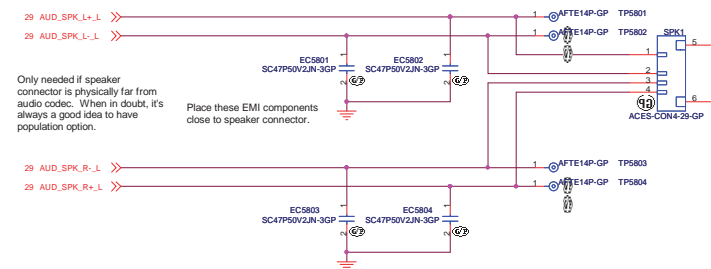


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

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Audio Jack LLW-1 / LGG-1	
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```
SSID = Flash.ROM
```

SPI FLASH ROM (4M byte) for PCH

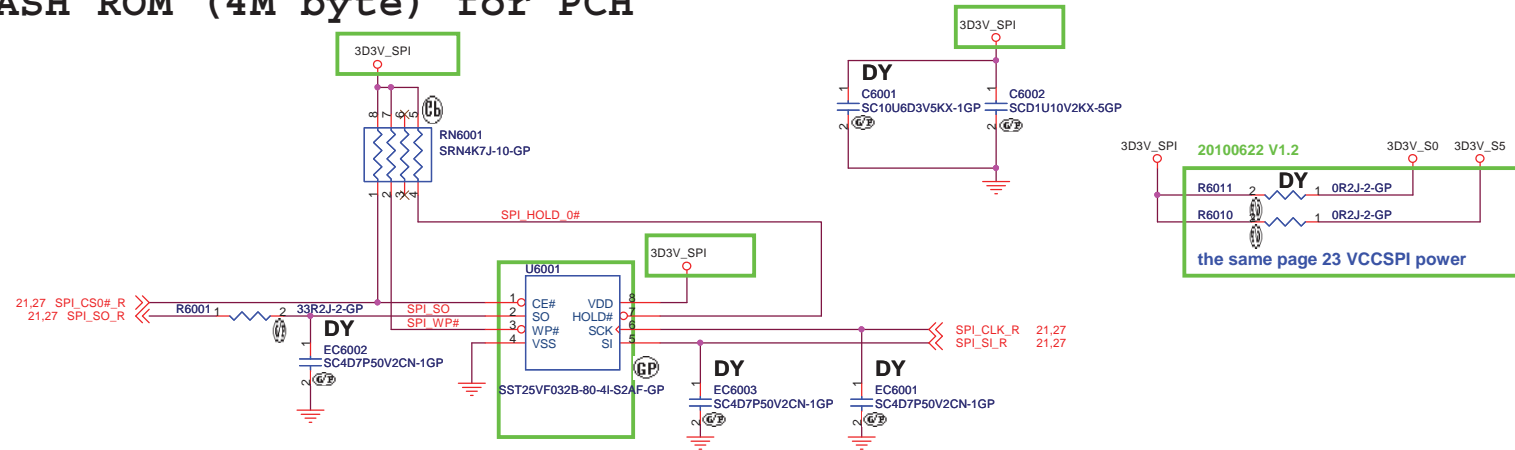


Table 60.1- SPI Serial Flash Memory multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
MXIC	MX25L3206EM2I-12G	N/A	72.25320.C01
WINBOND	W25Q32BVSSIG	N/A	72.25Q32.A01
NUMONYX	M25PX32-VMW6F	N/A	72.25P32.C01

SSID = RBATT

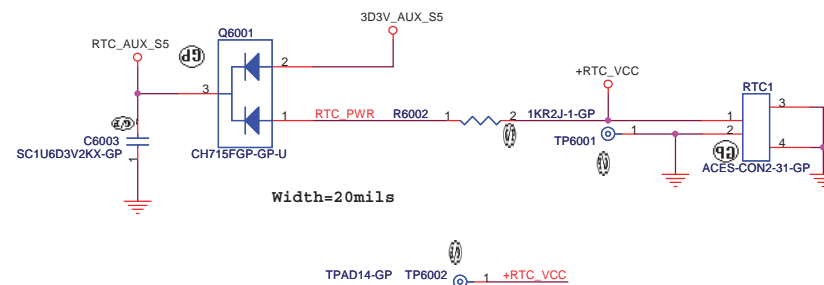


Table 60.2 - Schottky Barrier Diode multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	CH715FGP	N/A	83.R0304.D81
CHENMKO	BAS40CWGP	N/A	83.00040.R81
PANJIT	BAS40CW	N/A	83.00040.E81

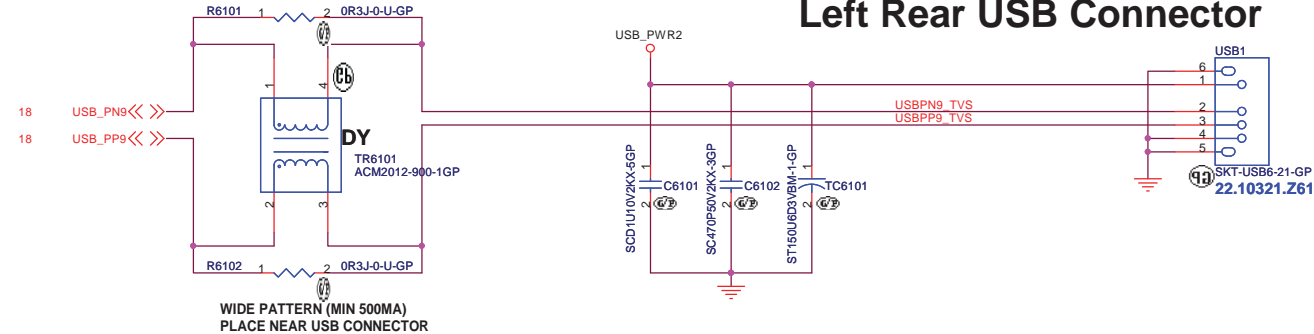
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Taipei Hsien 221, Taiwan, R.O.C.

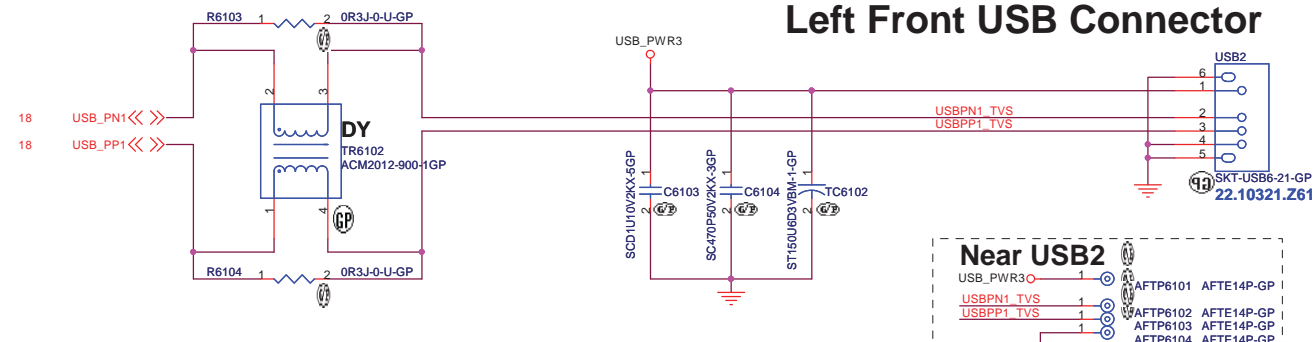
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Flash/RTC			
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USB Connector

WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR



Left Rear USB Connector



Left Front USB Connector

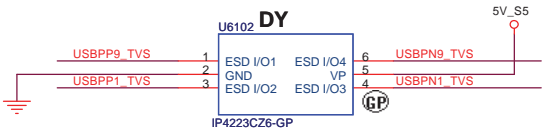
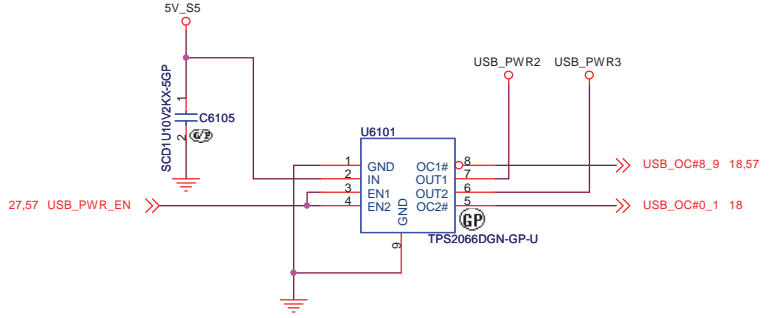
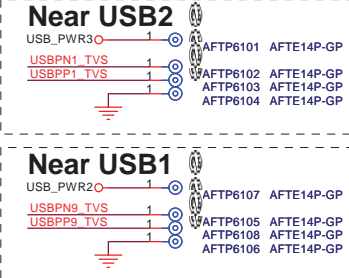


Table 61.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2066DGN	41R0511AA	74.02066.A71
TI	TPS2066DGN-1	N/A	74.02066.B71

Table 61.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

<Core Design>

緯創資通 Wistron Corporation
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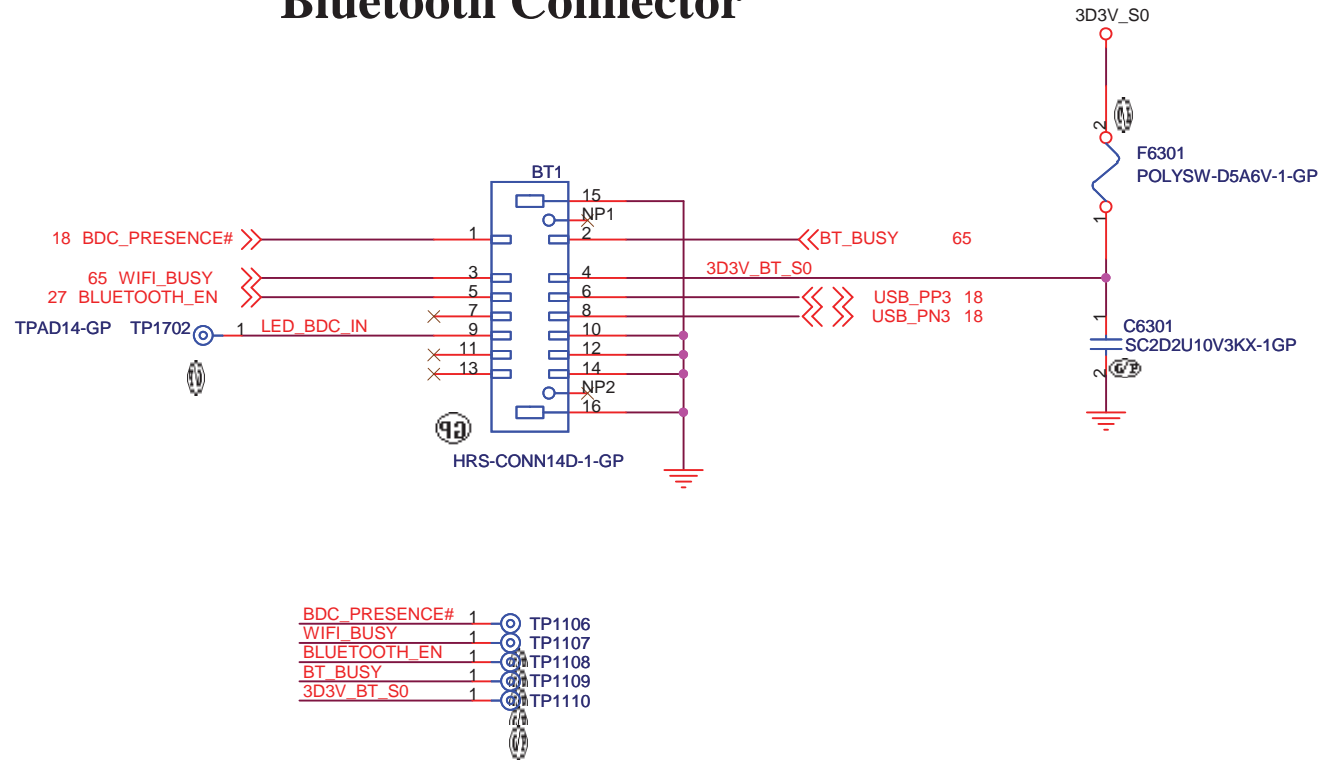
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Bluetooth Connector



<Core Design>

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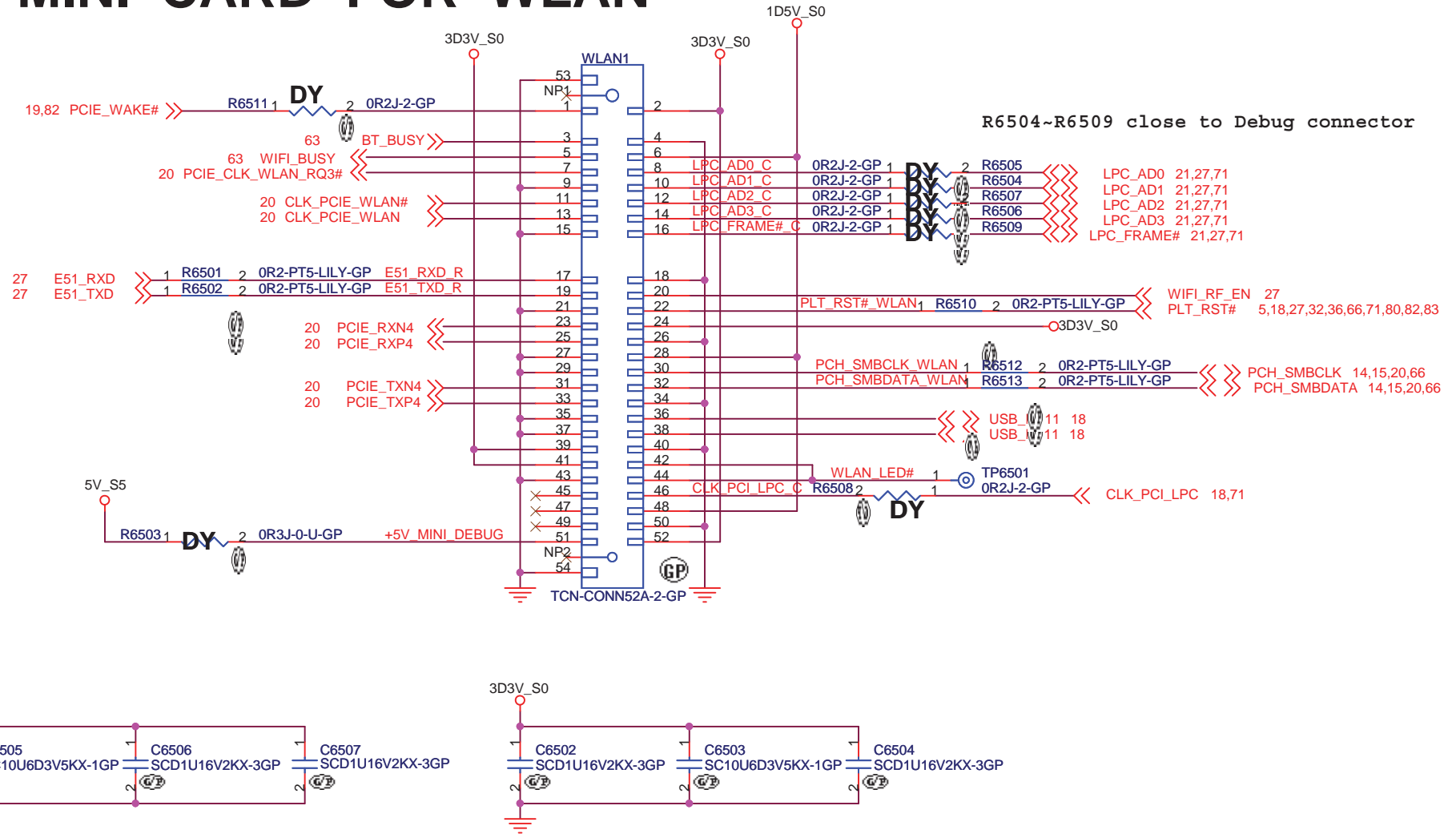
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HALF MINI CARD FOR WLAN



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

MINI CARD SLOT 1

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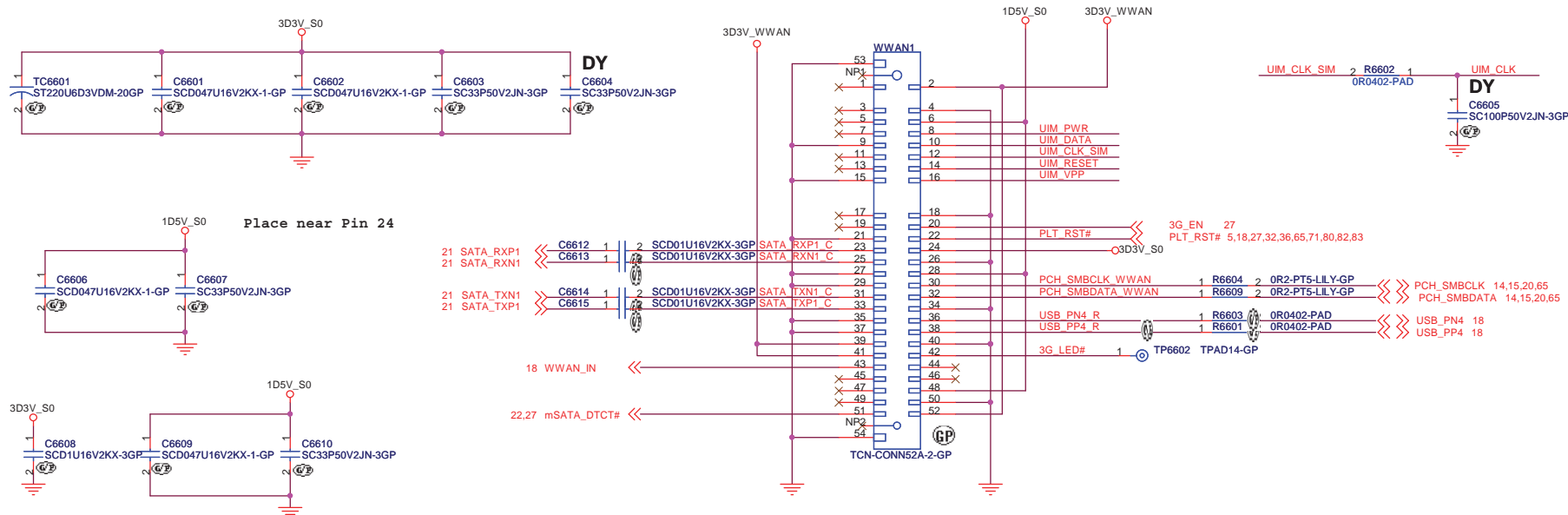
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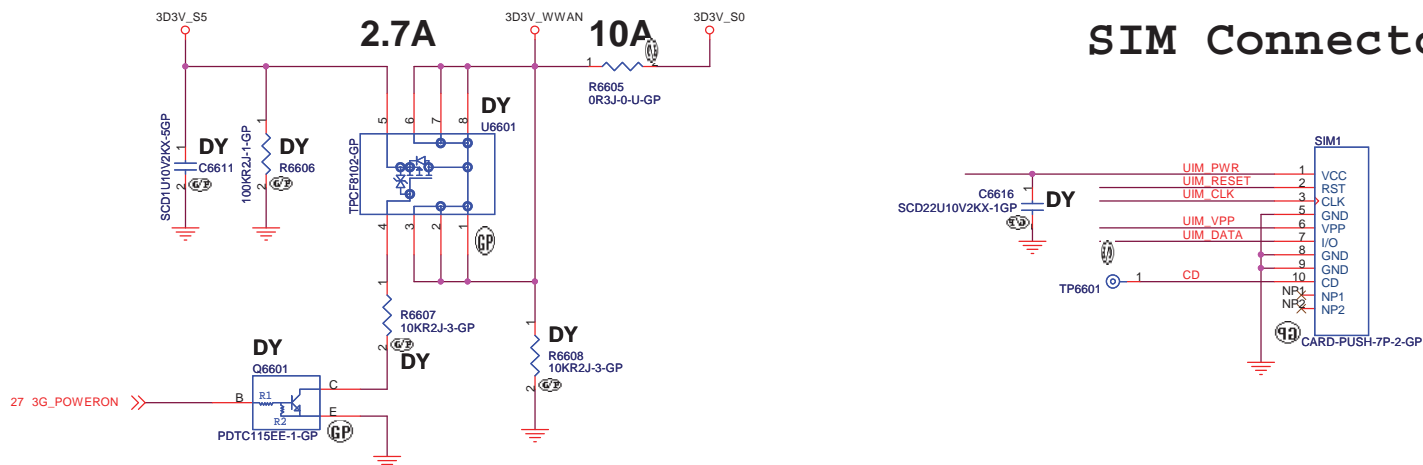
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Mini Card Connector(WWAN)

Place near MINI Card CONN



SIM Connector



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緯創資通 Wistron Corporation
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MINI CARD SLOT 2		
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Touch Pad Connector

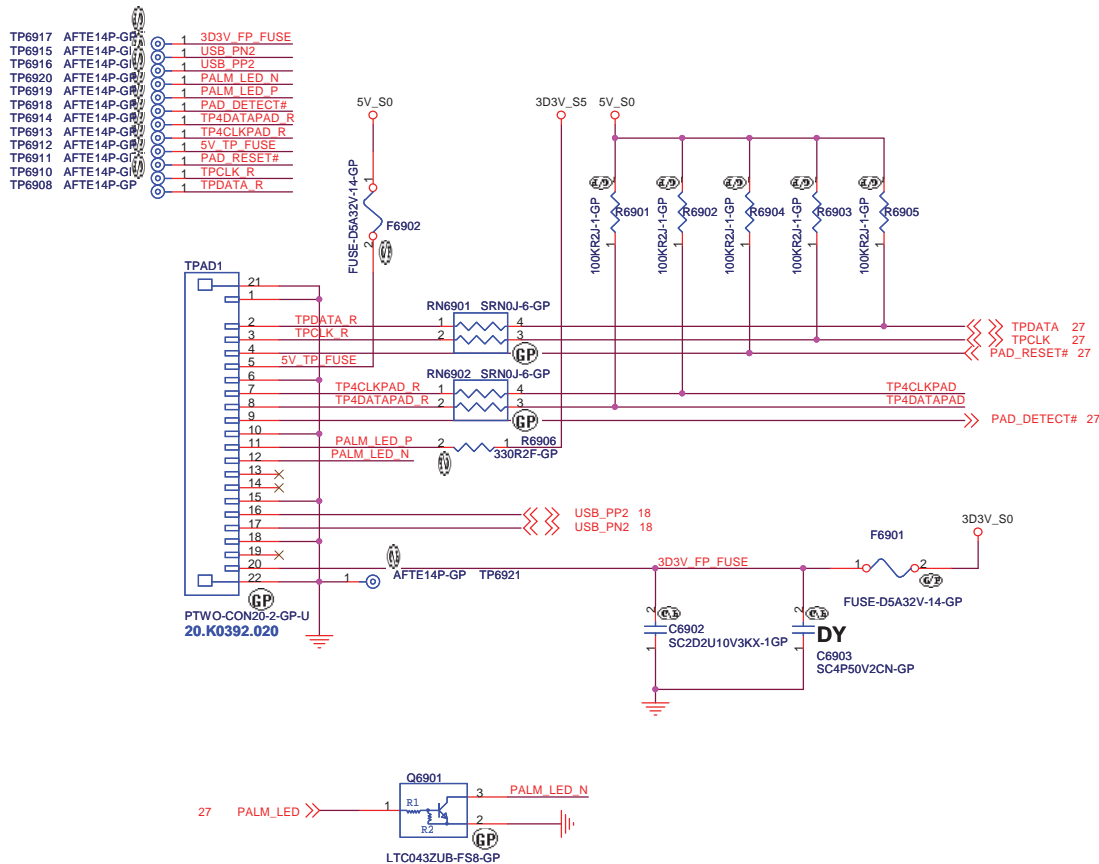
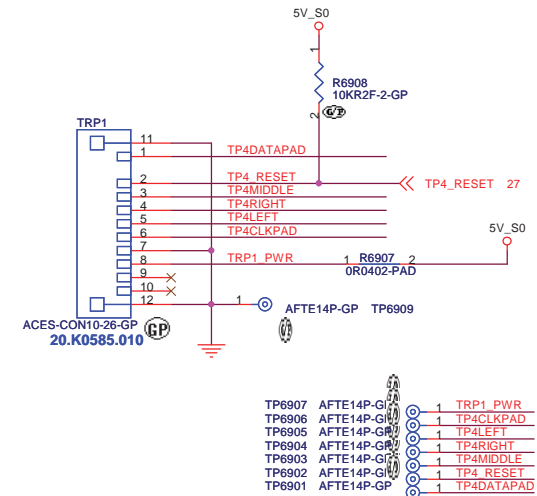


Table 69.1- Transistor multi-source

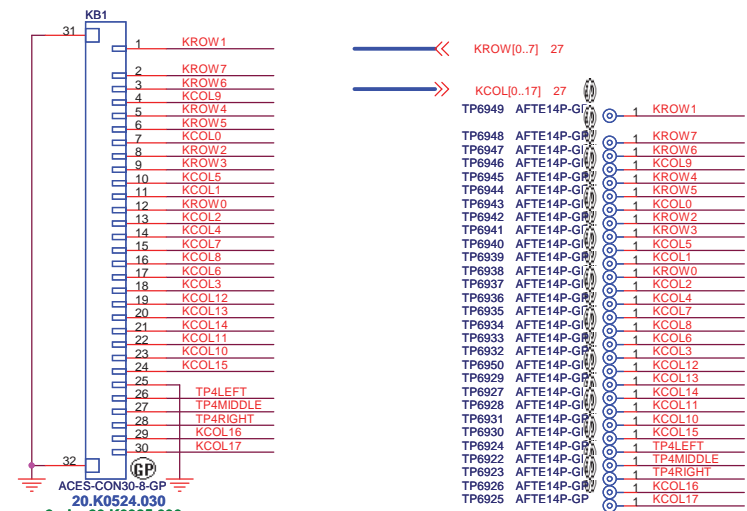
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ROHM	LTC043ZUB	N/A	84.00043.011
Panasonic	DRC5143Z0L	N/A	84.05143.011

WWW.AliSaler.Com

Track Point Connector



KeyBoard Connector



<Core Design>

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TOUCH PAD CONNECTOR			
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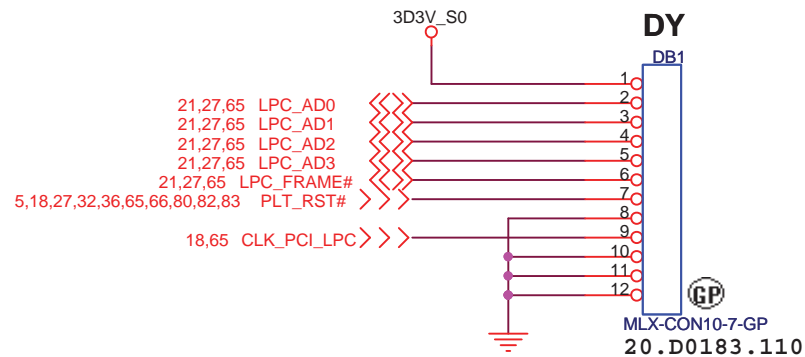
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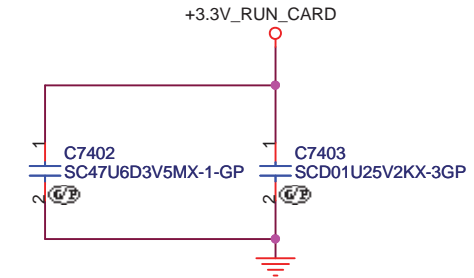
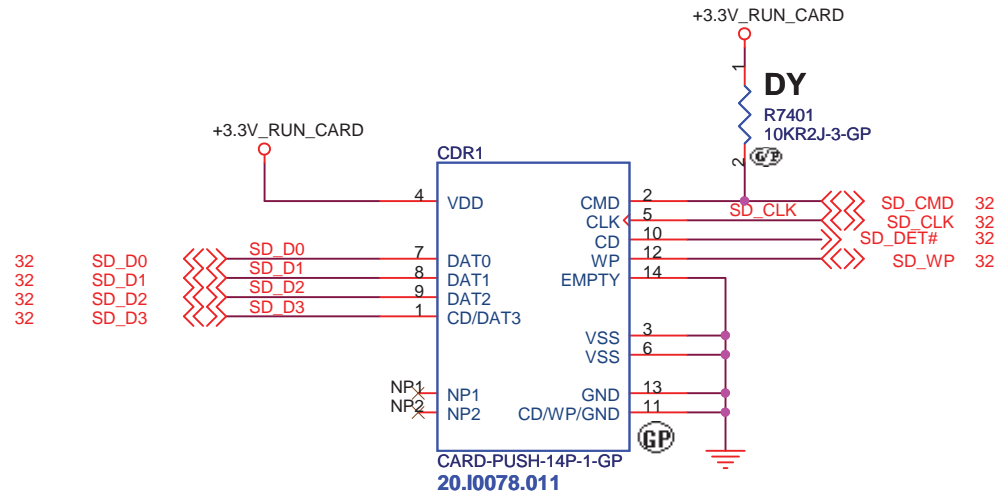
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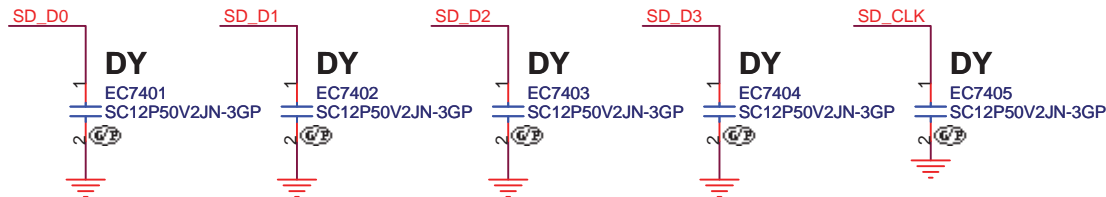
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Please apply Shield GND for SD_CLK signal between
R5U220 and SD Card Slot to decrease external noise.

Card Reader Connector



+3.3V_RUN_CARD trace = 40mil
C7402 lose CDR1



<Core Design>

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CARD Reader CONN		
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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

New Card

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-1

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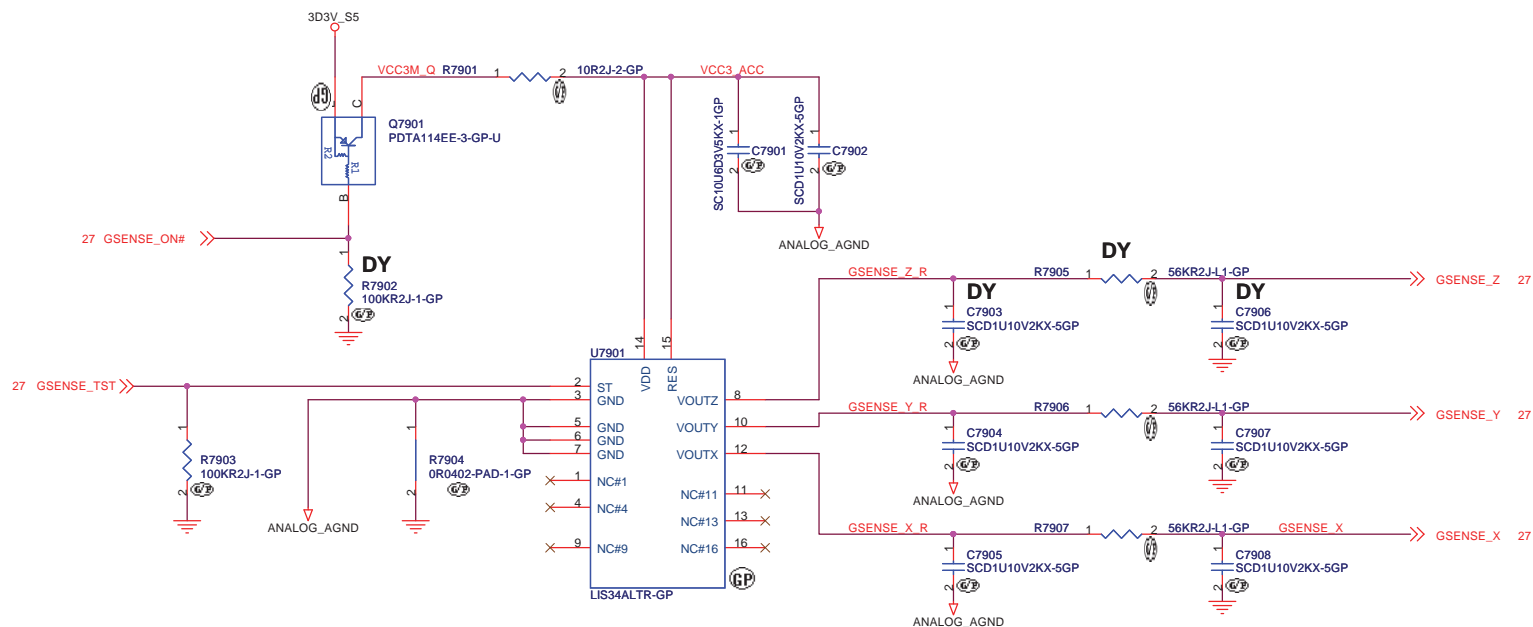
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Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
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G-Sensor



	LIS34AL	No Accel
	KXTC8-2850	
R7902	NO_ASM	ASM
R7903	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

- (1) Place C7904, C7905, Q7901, R7901, R7902, C7901, C7902, R7903, R508 close to U7901.
- (2) Avoid routing under DCDC switching area.

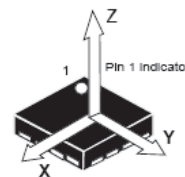


Table 79.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTA114EE	N/A	84.00114.H1K
ON	DTA114EET1G	N/A	84.DT114.B11
ROHM	LTA014EEB	N/A	84.00014.01H
Panasonic	DRA9114E0L	N/A	84.09114.A11

Table 79.2- Accelerometer multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ST	LIS34ALTR-GP	41R0828AA	74.00034.0BZ
ROHM-KIONIX	KXTC8-2850-GP	N/A	74.KXTC8.0BZ

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RFID

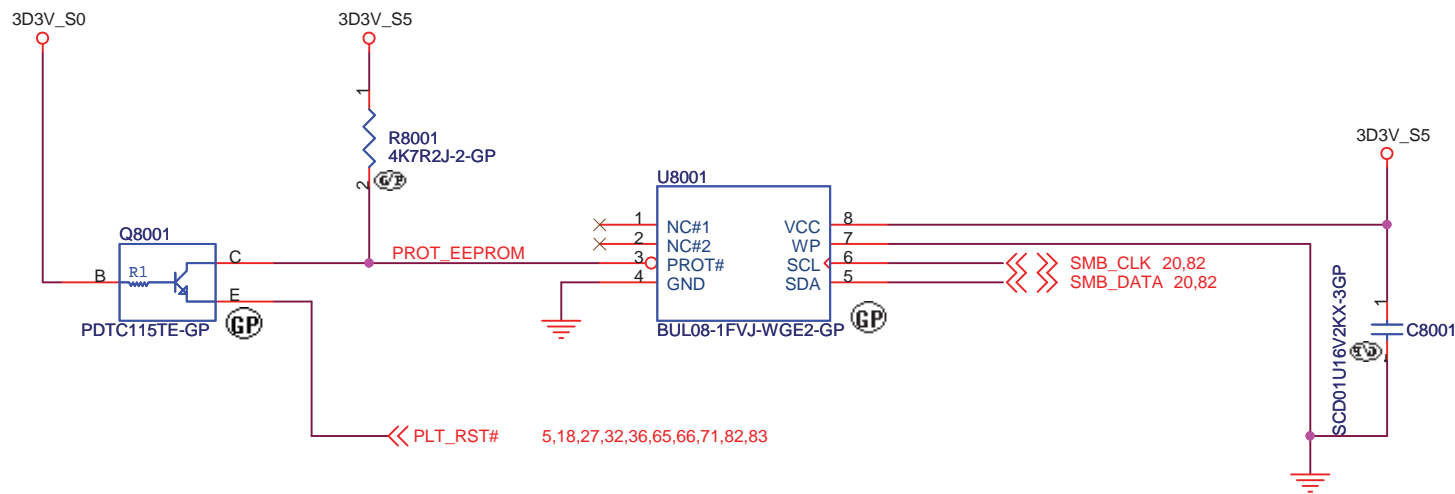


Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDT C115TE	N/A	84.00115.E1K
ROHM	LTC015EEB	N/A	84.00015.01H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE7SCAF05T-TLH-H	N/A	72.26C08.00R

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RFID					
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Document Number
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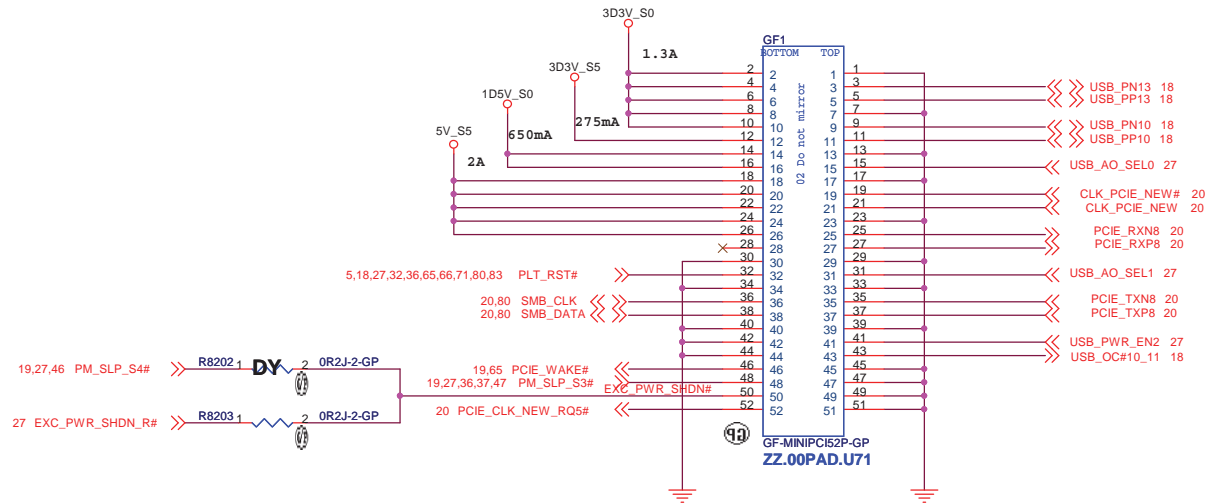
Rev
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Date: Tuesday, January 18, 2011

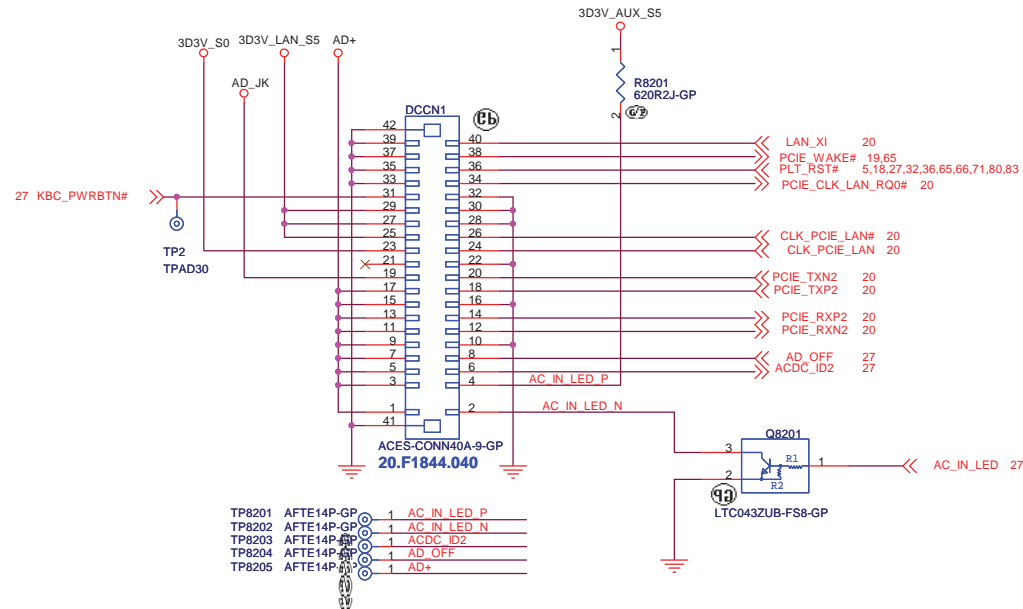
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TO EXP BOARD CONN



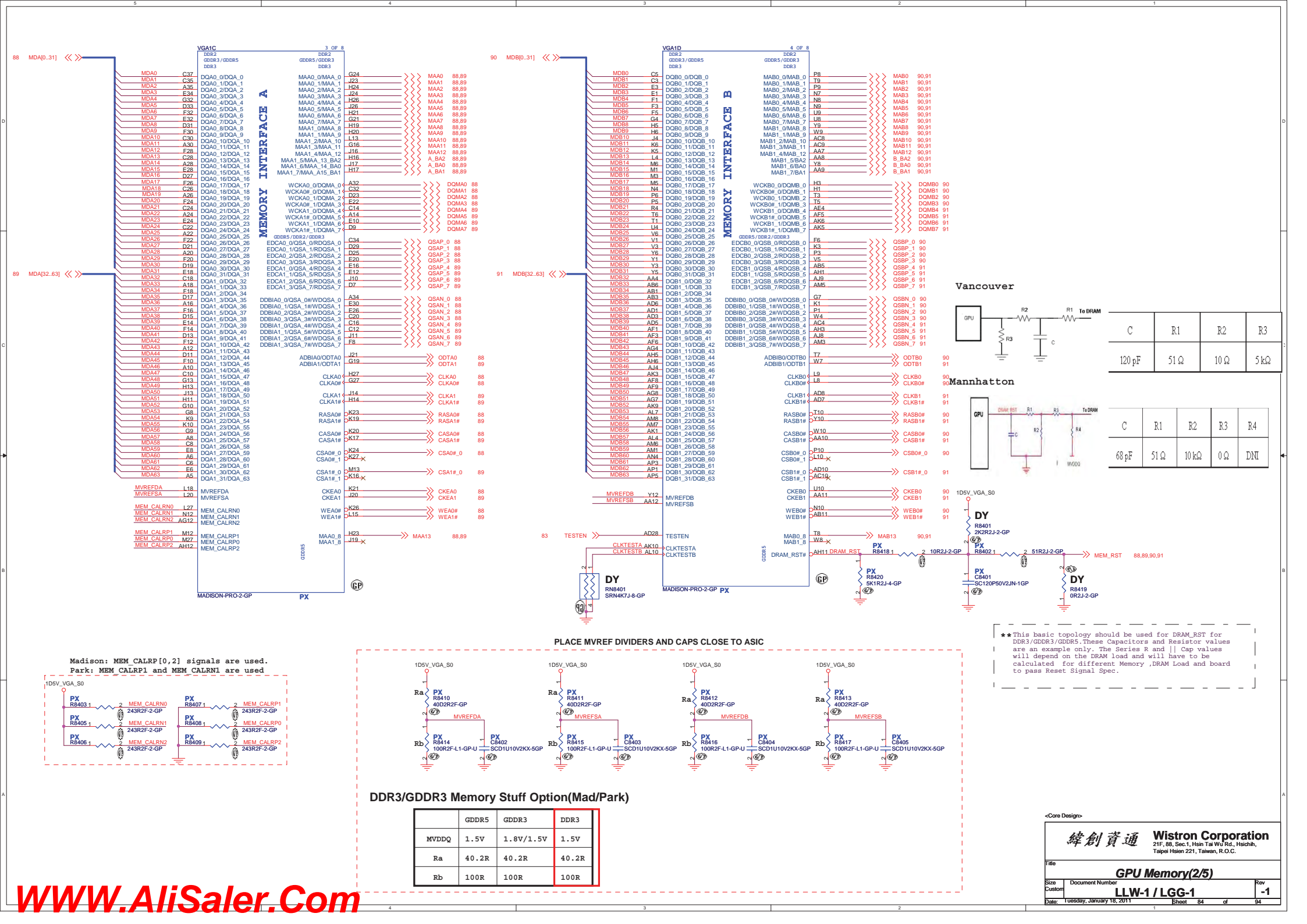
DC BOARD CONN



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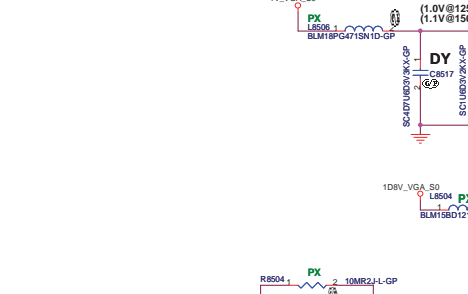
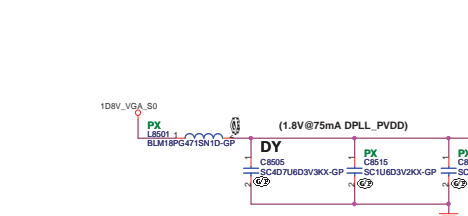
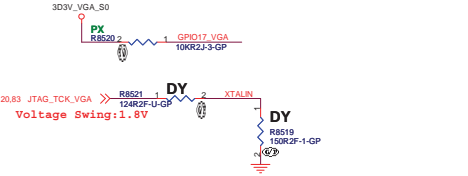
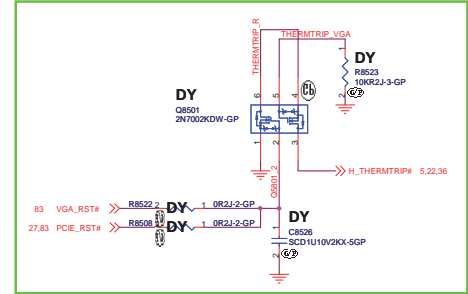
緯創資通 Wistron Corporation
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Title			IO Board Connector	
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DVPDATA [3:2:1:0] for VRAM type
selection B/W strap
Should provide VRAM Table for VBIOS request

DVPDATA [3:0]
0111 2Gbit Hynix-H5TQ2G63BFR-12C (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
1111 2Gbit Samsung-K4W2G1646C-HC12 (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
0011 1Gbit Hynix-H5TQ1G63BFR-12C (800MHz) (Whistler-LP 1G)
1011 1Gbit Samsung-K4W1G1646E-HC12 (800MHz) (Whistler-LP 1G)

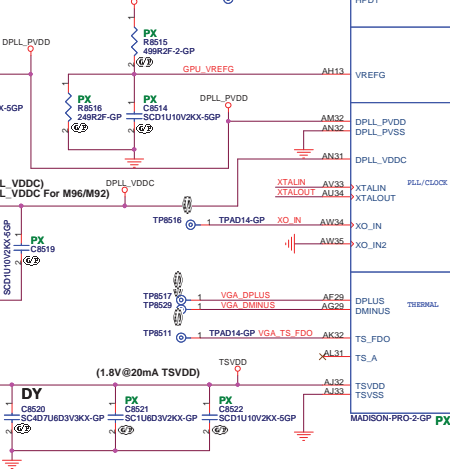
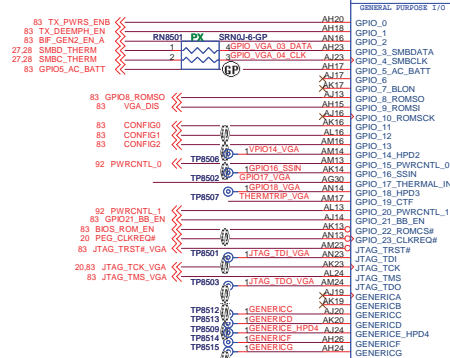
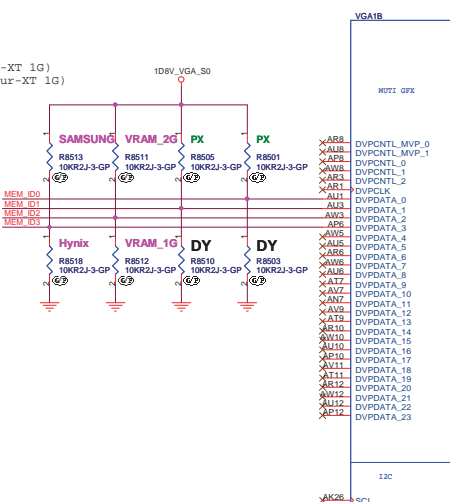


Clock Input Configuration - GDDR3/DDR3

a) 27MHz crystal connected to XTALIN or XTALOUT or

b) 27MHz (1.8V) oscillator connected to XTALIN or

c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

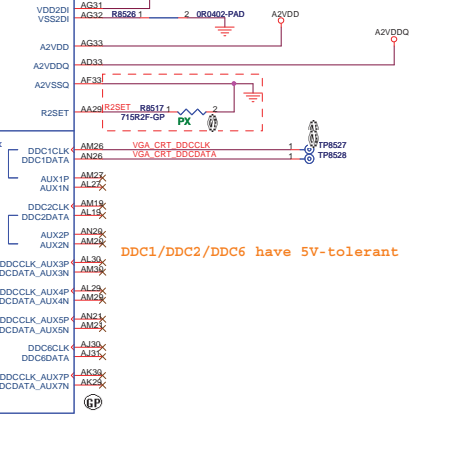
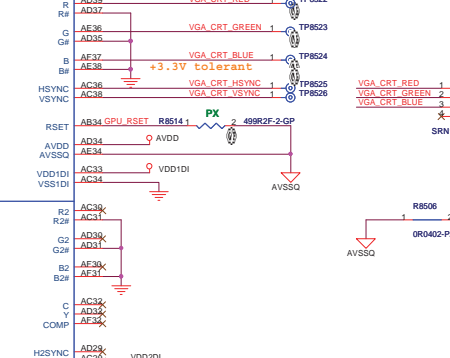


Clock Input Configuration - GDDR3/DDR3

a) 27MHz crystal connected to XTALIN or XTALOUT or

b) 27MHz (1.8V) oscillator connected to XTALIN or

c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

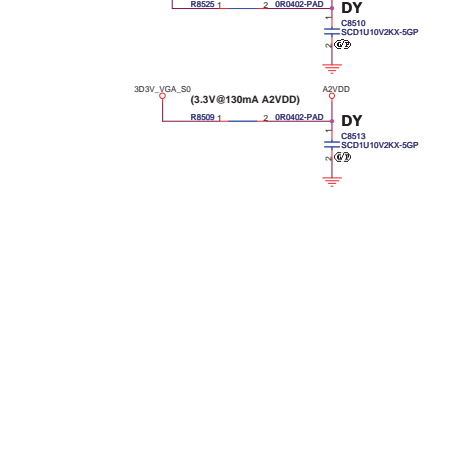
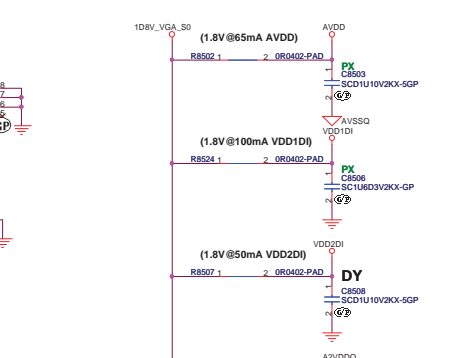
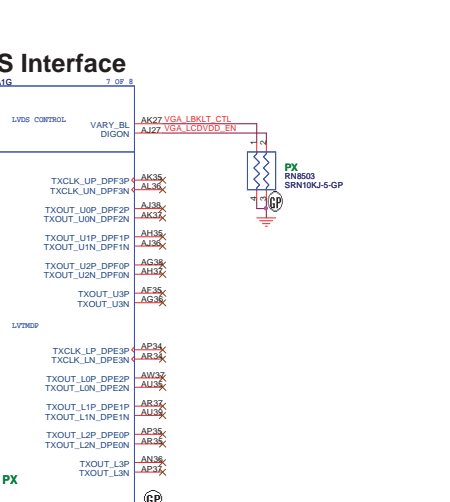


Clock Input Configuration - GDDR3/DDR3

a) 27MHz crystal connected to XTALIN or XTALOUT or

b) 27MHz (1.8V) oscillator connected to XTALIN or

c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

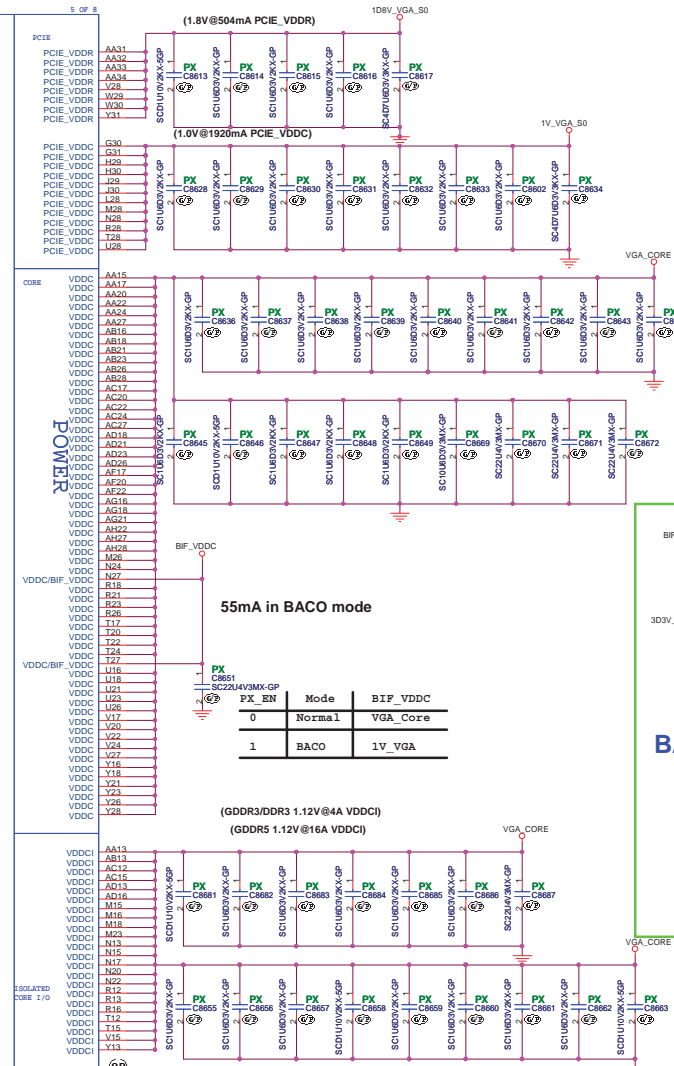


Clock Input Configuration - GDDR3/DDR3

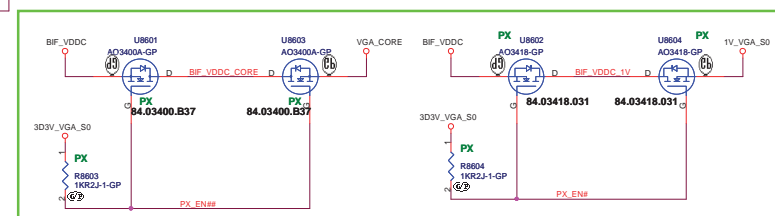
a) 27MHz crystal connected to XTALIN or XTALOUT or

b) 27MHz (1.8V) oscillator connected to XTALIN or

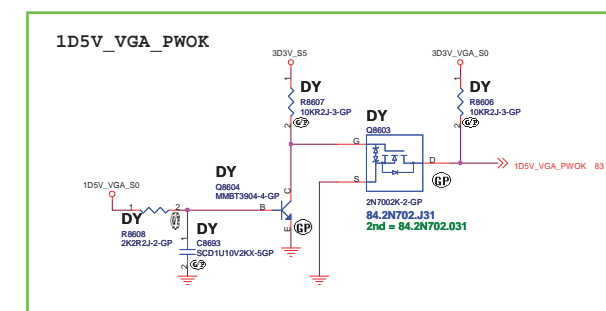
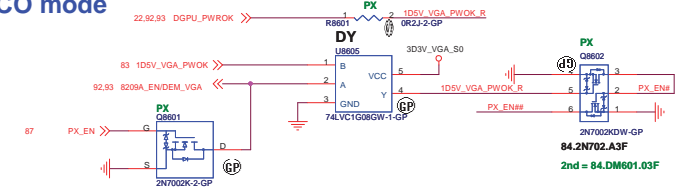
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

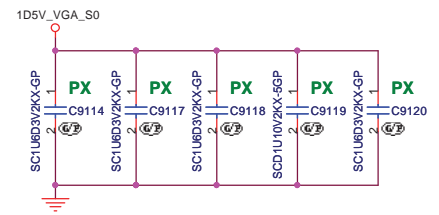
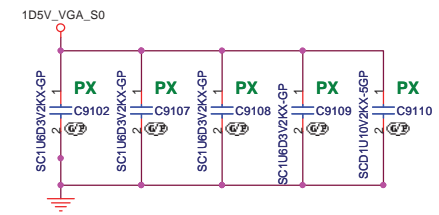
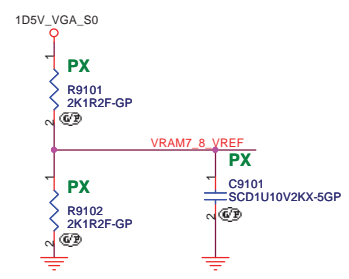
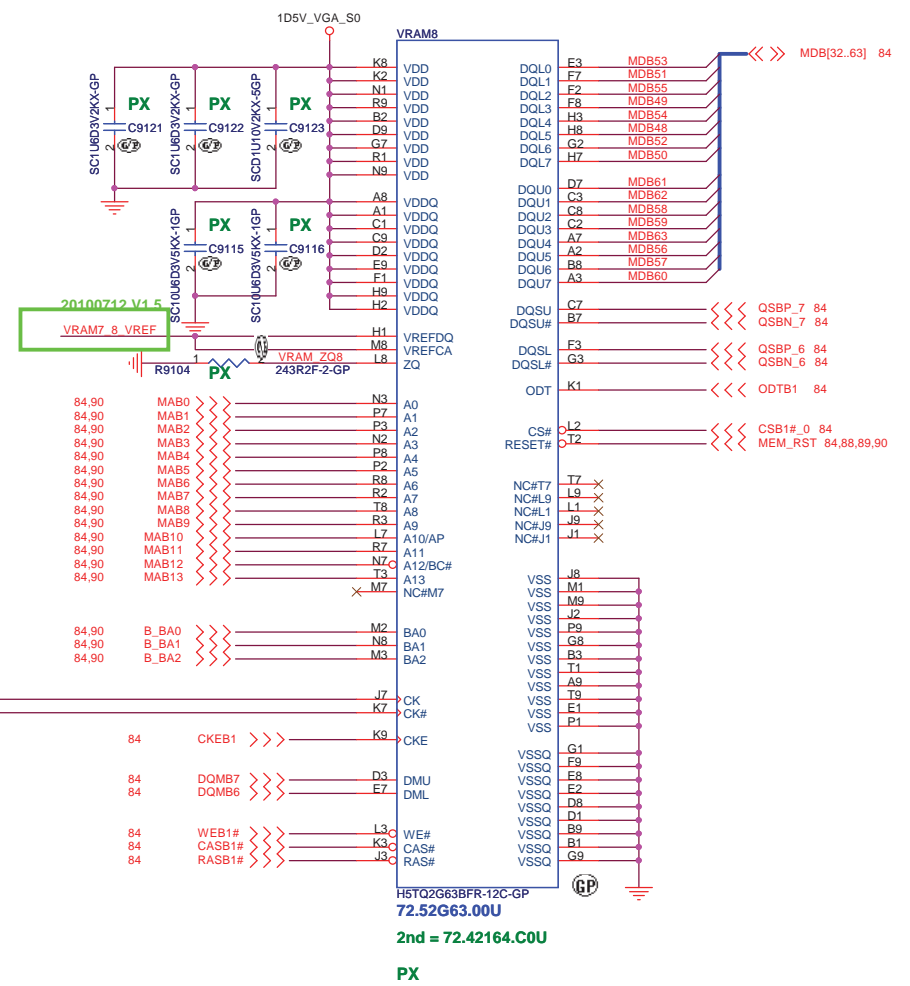
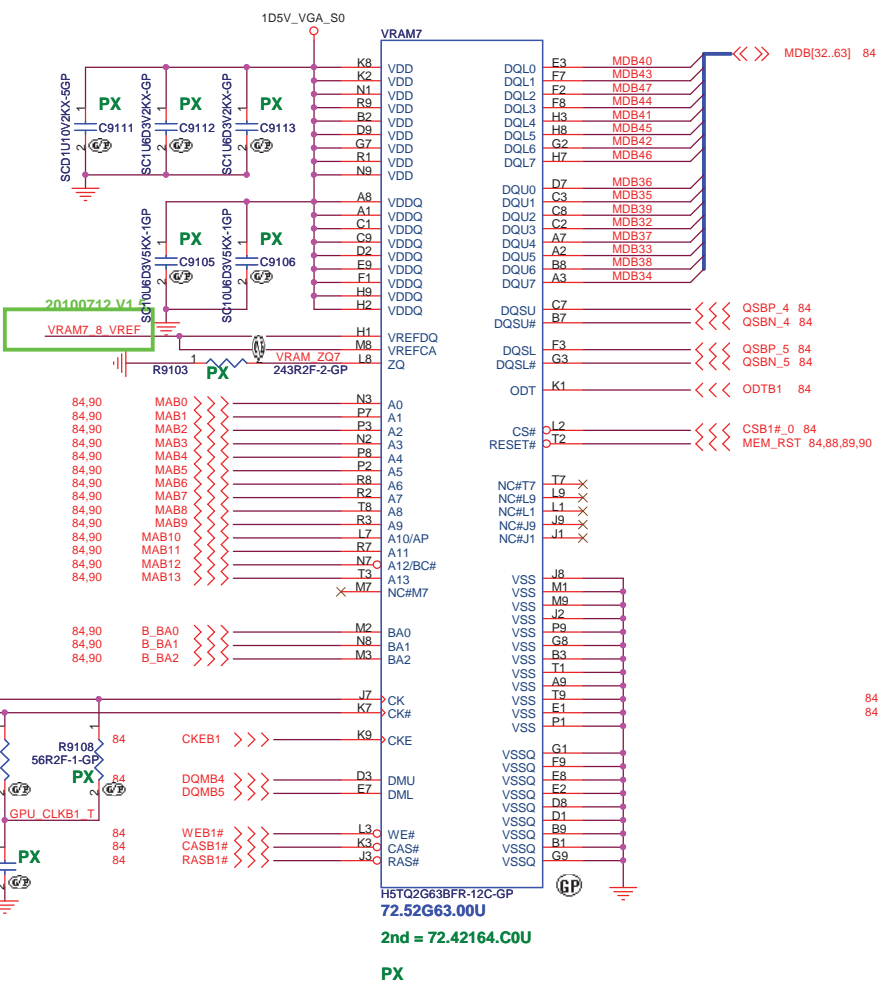


dgGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F-E]_VDD18, DP[D-A]_PVDD, DP[D-A]_VDD18, AVDD, VDD1, DL, A2VDDQ, VDD2DL, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F-E]_VDD10, DP[D-A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3, and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDC1	0.85~1.15V	OFF

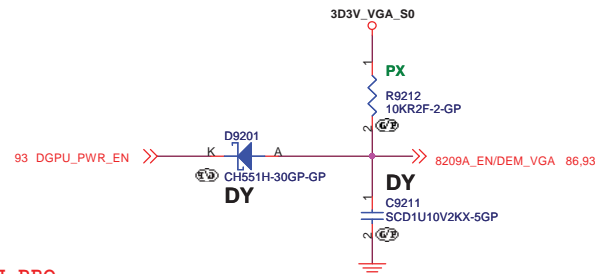
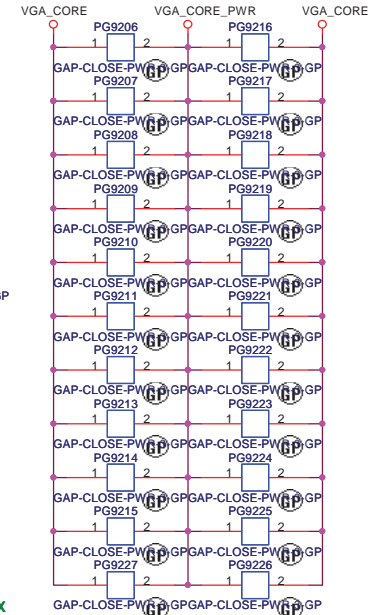
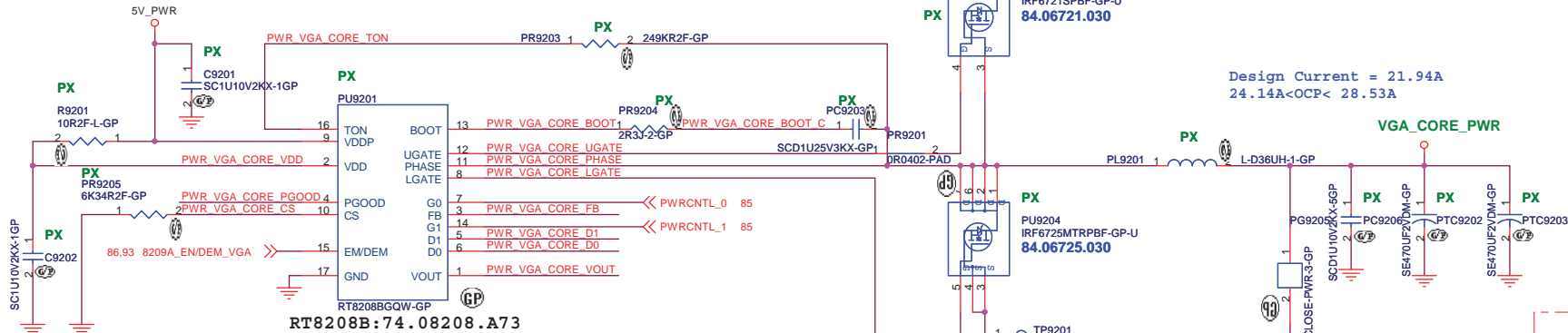
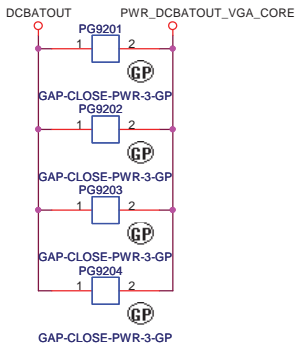


BACO mode

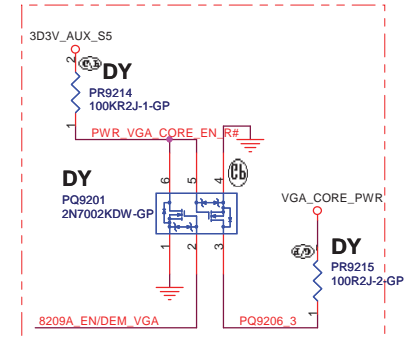
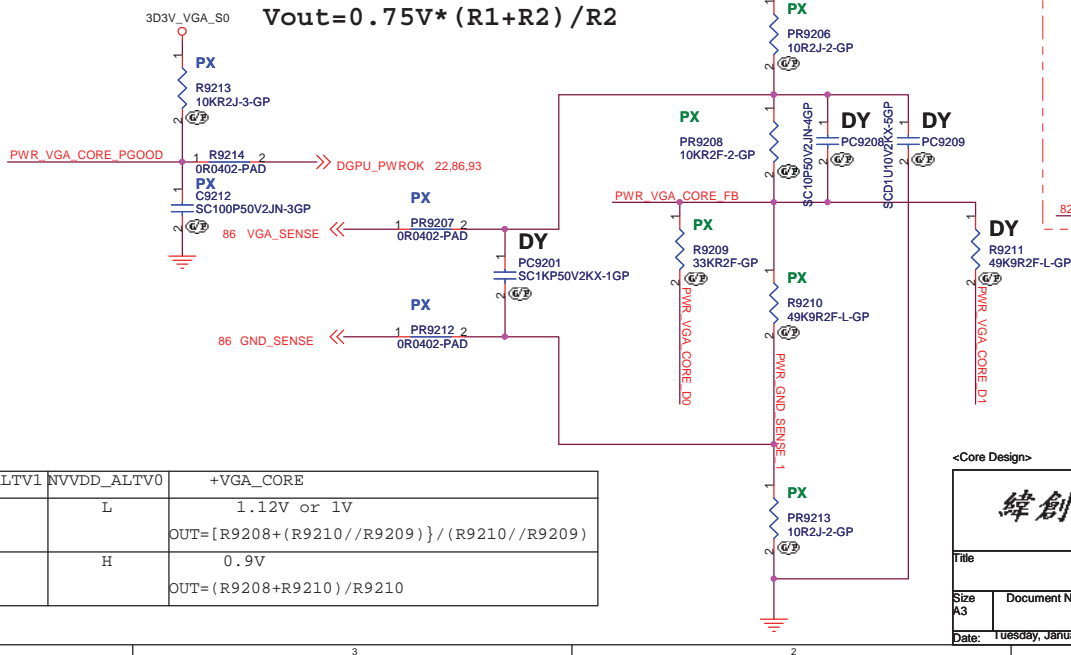




```
SSID = PWR.Plane.Regulator_GFX
```



$$V_{out} = 0.75V * (R1 + R2) / R2$$



MADSION PRO

Setting Vref Vout & Rfb-Top	Vref (V)	R9208	R9210	R9211	R9209
	0.75	10K	50K	50K	75K
VOUT (Target)	VOUT (compute)			VID1	VID0
1.150	1.150			0	0
1.050	1.050			0	1
1.000	1.000			1	0
0.900	0.900			1	1

```
WHIST => R9211 NO ASM.
SEYMR => whole ASM
```

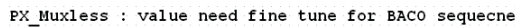
NVVDD_ALT1	NVVDD_ALT0	+VGA_CORE
H	L	1.12V or 1V OUT=[R9208+(R9210//R9209)]/(R9210//R9209)
H	H	0.9V OUT=(R9208+R9210)/R9210

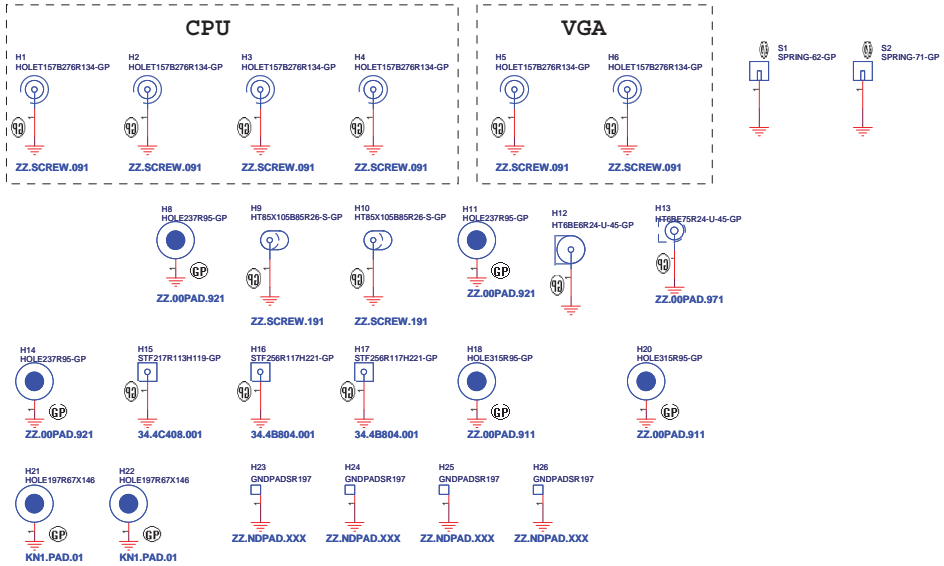
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RT8208B +VGA CORE			
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1D5V VGA S0





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